

Digital ASIC Fabrication

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Group #: sddec23-06

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Introduction

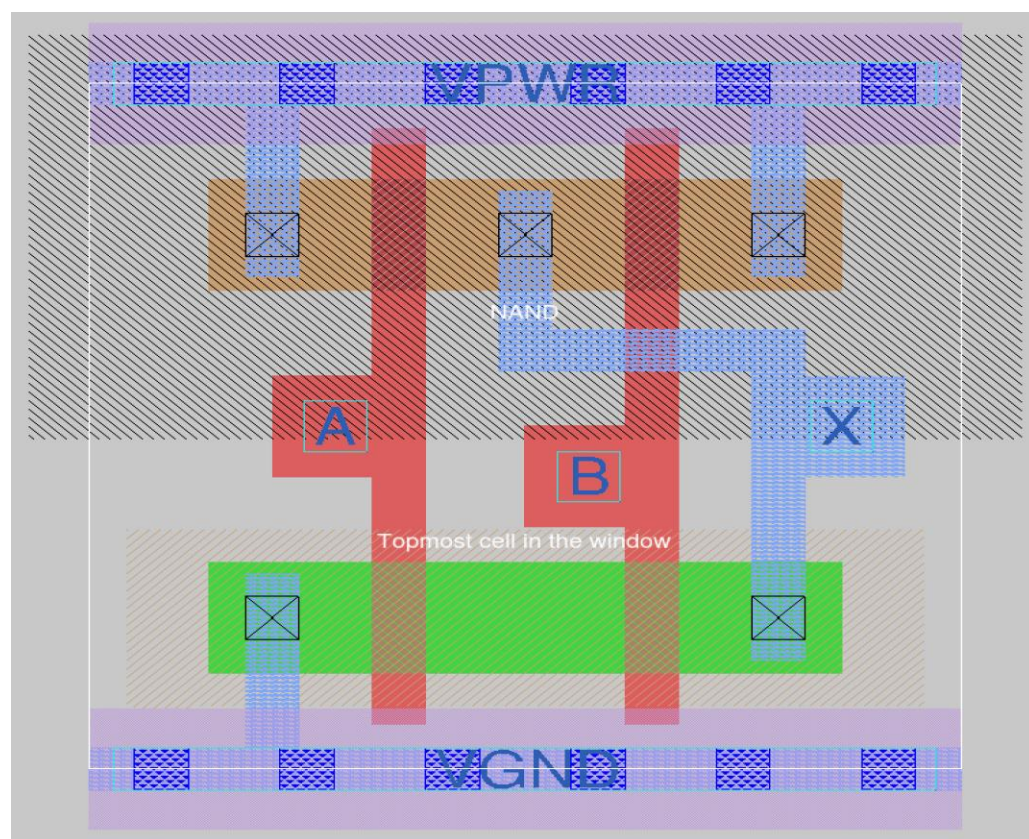
- Submit a custom digital ASIC
- High barrier of entry with lack of resources or knowledge
- Gain insight on the Open MPW fabrication process

What is Open MPW?

- Collaboration between Google, eFabless, and SkyWater foundry
- Allows for groups to create and submit open-source ASICs for FREE
- Typically expensive, makes more accessible to users without proprietary tools

Design Requirements

- Create a design that tests different aspects of manufacturing process
- Meet the restrictions placed by the eFabless Open MPW submission
 - size available on chip
 - pass given precheck tests
 - 38 I/O pins
 - 128 Logic Analyzer pins



Users and Purposes

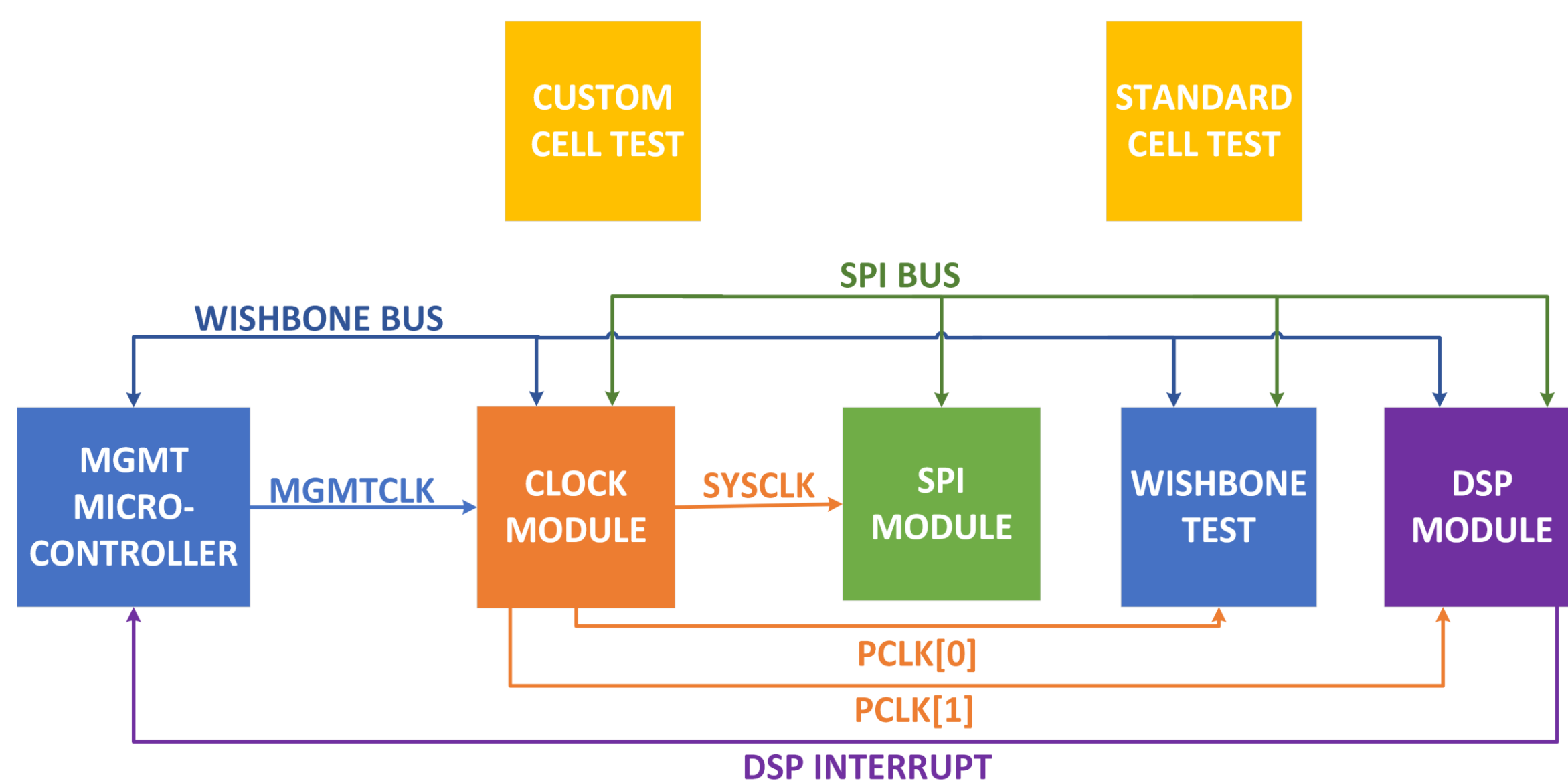
- Users
 - Future Senior Design groups
 - Research groups
 - Open-Source community
- Purpose
 - Gain insight on tooling
 - Reproduce work in more efficient manner

Open-Source Tools Used

- EFabless Caravel Wrapper
- SkyWater 130nm OpenPDK
- OpenRoad
- GTKwave
- Klayout
- Magic
- XSchem

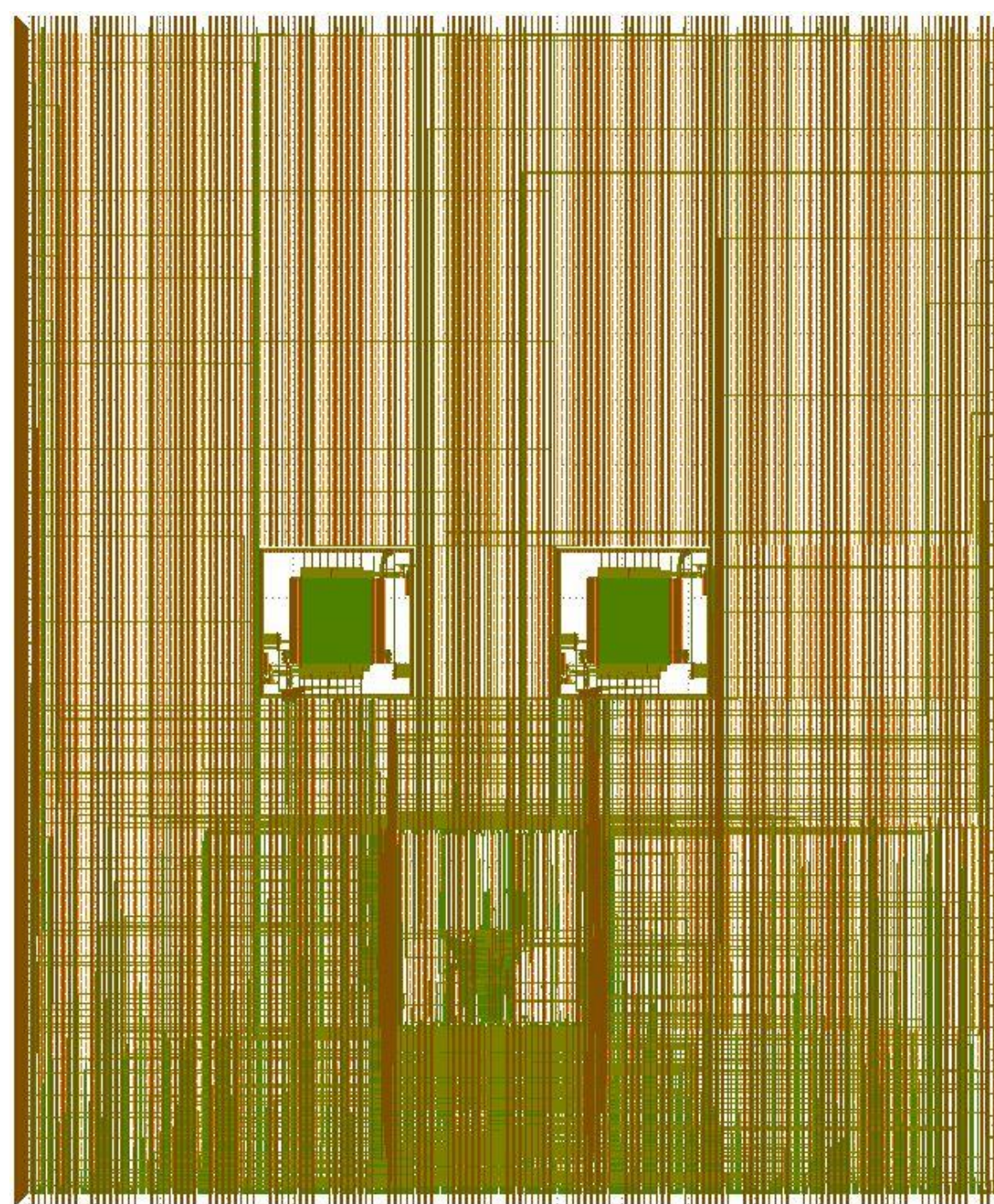
Design Approach

- Modular design with multiple independent functional units
- Communicates over provided Wishbone Bus and designed SPI
- Synthesize behavioral Verilog, custom cells, and memory macros
- Learn more about hardening process for varying designs



Technical Details

- Standard Cell – implement a AND cell given by the PDK
- Custom Cell – create a custom NAND cell with Magic to be made
- Wishbone Test – Verify the provided Wishbone bus in the user area
- Backdoor SPI – Communicate with other modules via external I/O
- DSP Accelerator – Convolution accelerator for dense gate count
- Clock Gating – Choose between wishbone clock or SPI clock



Testing

- RTL simulations of individual modules using Verilog
- Gate level simulations with synthesized design results
- Signoff simulations with synthesized and placed macros
- Integrated top level verification using Verilog and C testbenches
- Run eFabless Precheck for final submission approval
 - Includes DRC, LVS, and Complexity Checks

