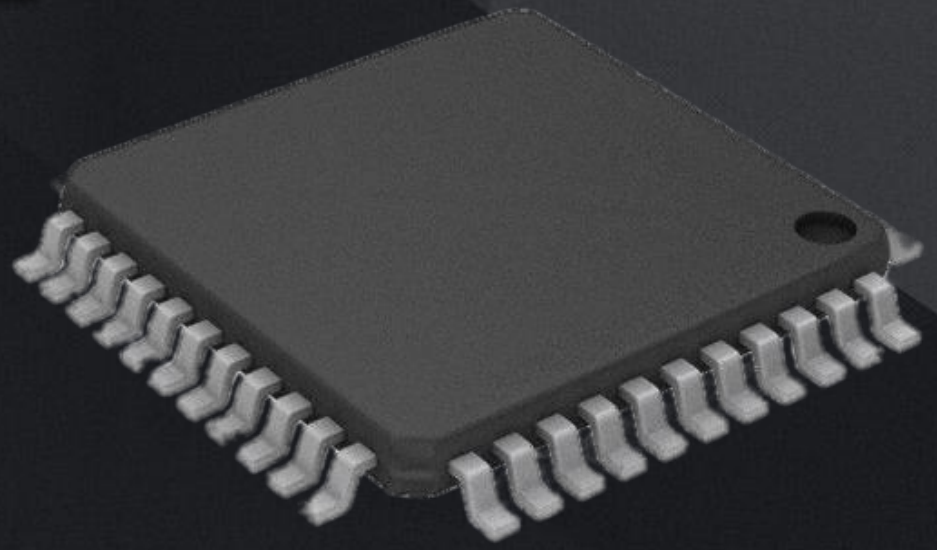

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Digital ASIC Design
Faculty Panel Presentation

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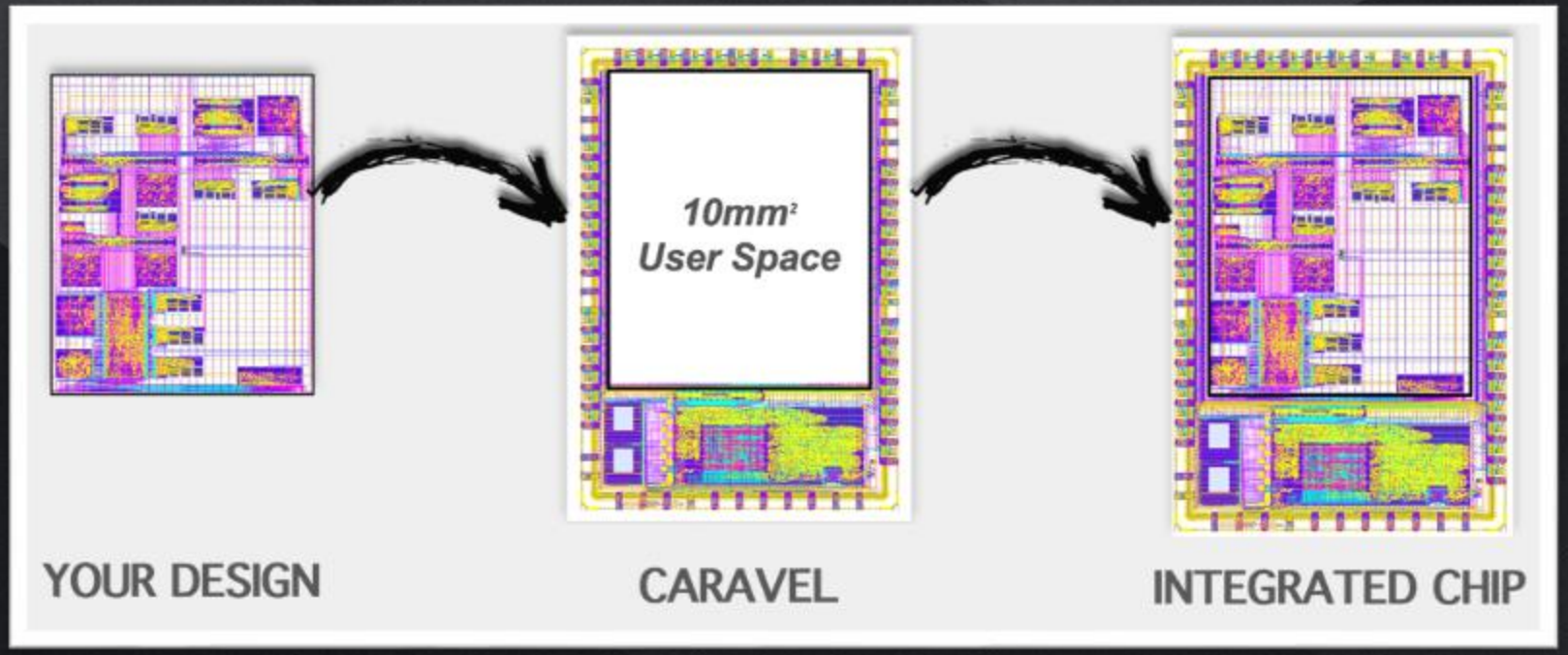
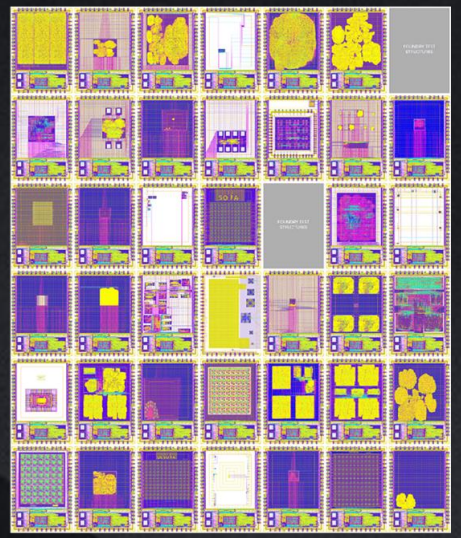
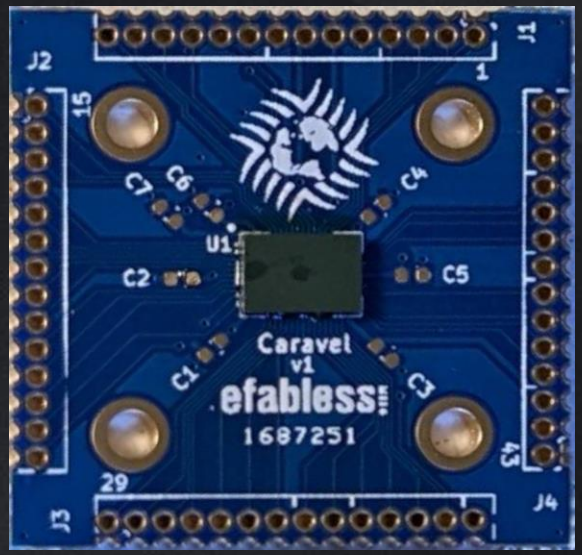
Overview

- ASIC Design
- OpenMPW (eFabless)
- Open Source

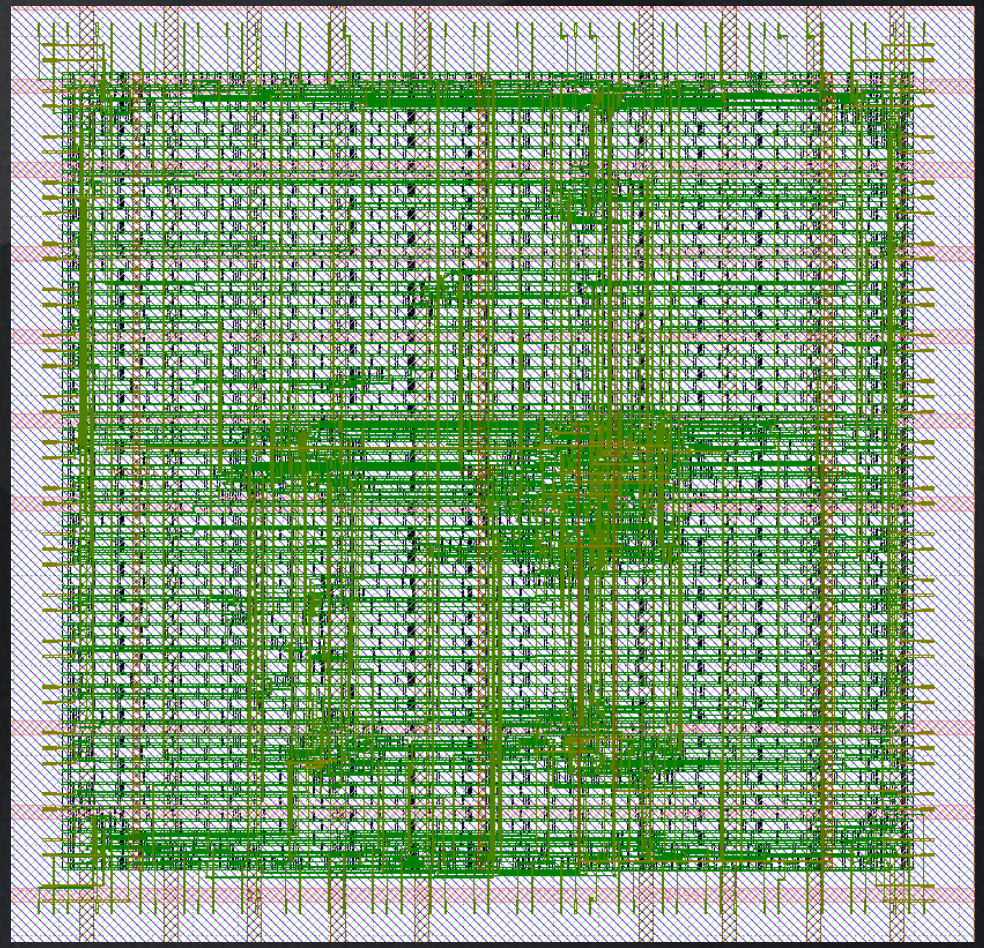




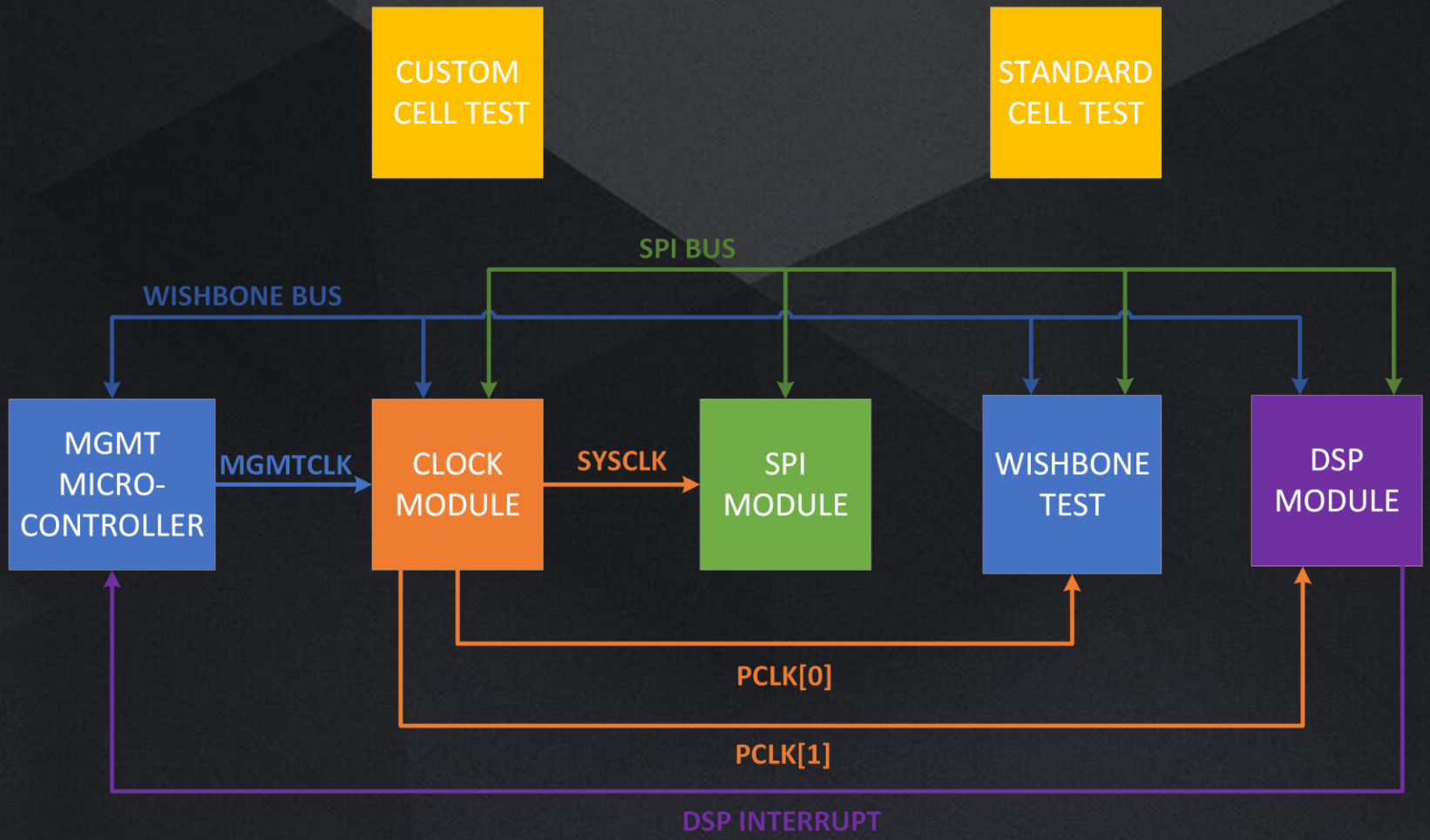


Project Goals

- Submit a functional ASIC to eFabless
- Test the limits of the sky130nm manufacturing process
- Modular design
- Implements failure resistance to ensure at a minimum a partially working design



Top Level Design



Current Status and Schedule

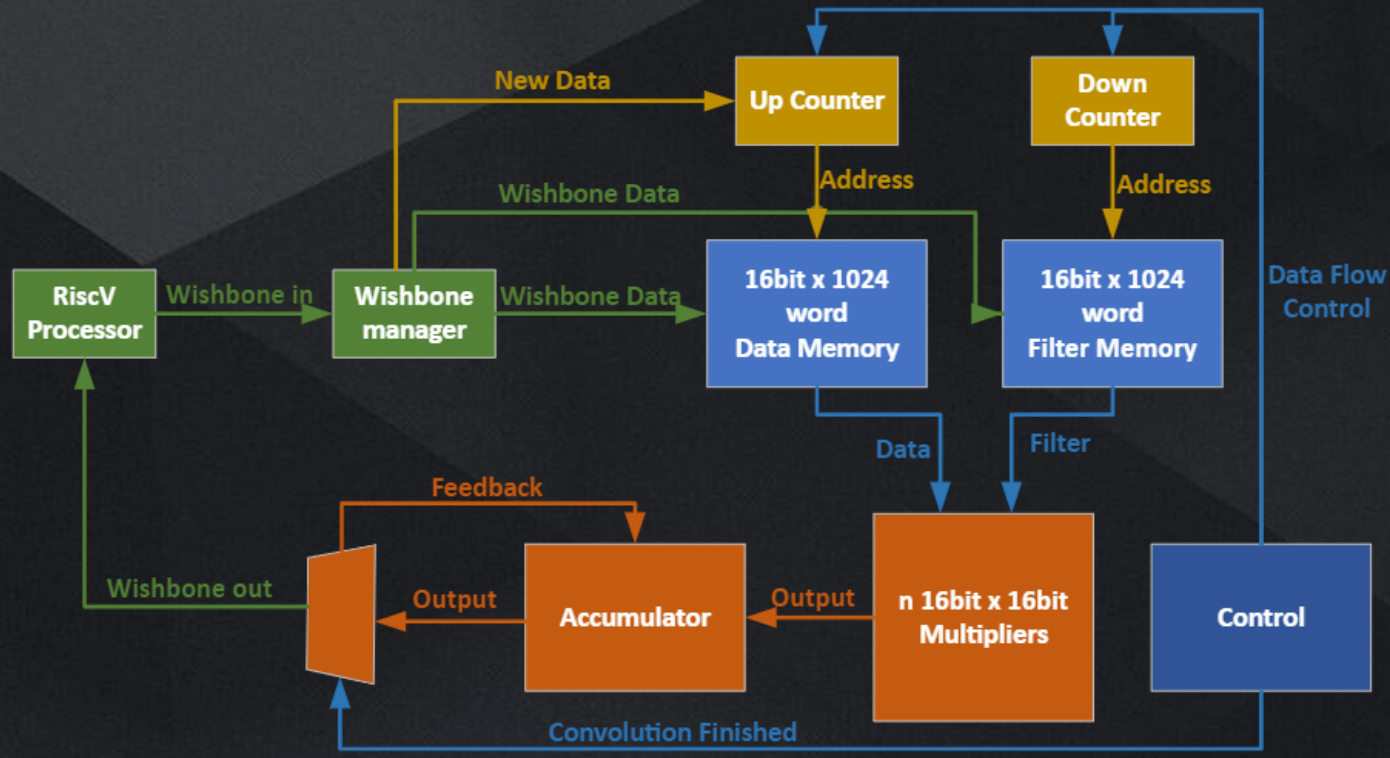
Task	Deadline	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Install the open-source tools and simulate sample code	2/19/2023												
Define our project specifications	3/19/2023												
Draw out a top-level diagram of the user area including each individual module	3/26/2023												
Draw out detailed implementation of each module	4/2/2023												
Write initial Verilog implementation of each module	5/14/2023												
Test and iterate using RTL simulations	8/20/2023												
Join modules together and verify final design as they are completed	8/27/2023												
Test and iterate using RTL simulations	9/22/2023												
Verify using gate-level simulation	9/22/2023												
Verify submission using the provided verification tools	10/1/2023												
Submit to MPW Shuttle	10/8/2023												
Create Software to run on embedded microcontroller	10/22/2023												
Create Documentation and bring up plan to test returned project in the future	11/3/2023												

Big Design Milestones

- SPI module has been finished and fully tested
- DSP module has been finished and fully tested
- Standard Cell module has been finished and fully tested
- Created first CMOS Inverter in Magic (custom cell)
- Top level test bench has been created to test module integration

Technical Challenges

- Digital implementation of the DSP module
- Usage of the open-source memory tools
- Usage of open-source custom cell design tools



Questions?