EE/CprE/SE 492 Bi-WEEKLY REPORT 6

Digital ASIC Fabrication

11/9/2023 – 11/22/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breedings

Past Week Assignments

- Gregory
  - Test DFF manual placement coordinates, help in the final hardening/bring up plan
- Jake
  - Help integrating prehardened macros (custom DFF, SRAM, clk mux)
  - Document hardening efforts and precheck process
  - Discuss next steps AFTER hardening success (more functional testing would be cool)
- Will
  - Rework project to have memory instantiated in the user project wrapper
  - Get the memory to harden by itself in the top level.
  - Get all the previously hardened modules along with the dsp module to harden with the memory.
- Cade
  - Confer with group to discuss solutions from Saturday and discuss next steps

Meeting Notes from Previous Week with Dr. Duwe

11/15/23

Updates from us

Whats the status?

- RAM hardened, all behavioral in
- All but NAND custom cell and clock MUX in design
  - Ask why the PDK changed for clock MUX
- Rough draft for poster complete
- Jake went through design document and highlighted areas to change
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Schedule

- Duwe: Should have practice presentation before

Poster Feedback

- Take up less white space and junk space for things like our names
- Tighten up footer size
- Right balance of figures and text
- Double check all required info

Deliverables

- What are our deliverables?
- Some have a hard deadline, some do not
- No hard deadline for technical deliverables
- Work back from external presentation and poster that we want to show off for

From Duwe:

- What should the focus be?
  - Be positive in context to project
- Some of deliverables are expanding in house technical capabilities
- What we can show is that we have added significantly to knowledge base here positively
- Might say "we looked back at open source projects", determined a lot of them wont actually work
- Focus on user guide as well as extension of signoff
  - Dug more into post layout issues
  - May or may not be caught by precheck

TODO

- Meet in two weeks and do presentation with Duwe
- Schedule and prepare presentation EARLIER
- "This is how we did signoff", STA and SPF
  - Goal is to show off that we have taken the process very seriously and if in industry
- DEFINE WHAT PRECHECK IS
  - What does it do?

        - DRC checks, LVS checks, etc
    - Prepare presentation Wednesday after break with Dr. Duwe

Bi-Weekly Progress

- Gregory
    - Fixed NAND issues in precheck DRC
    - Fixed NAND/clkmux issues in precheck LVS
    - Added clkmux to design pulled from the old hdll pdk
    - All custom cells pass precheck completely
    - Added notes to the user guide
- Jake
    - Helped design poster presentation first draft
    - Documenting hardening process
    - Defined new IO and LA pin assignments in spreadsheet
    - Update top level Verilog testbench with new IO and LA ports
- Will
    - Redesigned DSP unit to take the memory out
    - Moved memory to user project wrapper
    - Hardened and prechecked new DSP orientation
    - Added in all remaining modules to top level user proj final and wrapper once they had been individually tested
    - Hardened final design
    - Prechecked final design
    - Design is complete
- Cade
    - Help with poster and revise
    - Help with design document revision
    - Looking at presentation for things to change

Individual Contributions

Team Member	Contribution	Hours per report	Total Hours
Jake Hafele	Hardening efforts, updating pinouts, top level testbenches	15	175
Gregory Ling	NAND and clkmux fully working!	50	166
Will Galles	Got DSP and memory to actually harden. Got final design to hardne and paass precheck	40	200
Cade Breeding	Documentation, including poster and design doc	15	110

Plans for Upcoming Two Weeks

- Gregory
  - Write C tests and user guide notes
- Jake
  - Run RTL, GL, and SPF simulations on top level user project wrapper module
  - Document top level simulation results
  - Help with updating design document/presentation
  - Celebrate being done (???)
- Will
  - Aid with the verilog test benches
  - Aid with the C tests and bring up plan
  - Rework my portion of the design doc
  - Help polish the poster
  - Help with the presentation
- Cade
  - Help with c test
  - Revise poster
  - Revise design doc
  - First draft of presentation