EE/CprE/SE 492 Bi-WEEKLY REPORT 5

Digital ASIC Fabrication

10/26/2023 – 11/8/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breedings

Past Week Assignments

- Gregory
  - Import the custom DFF into the wrapper and get it to harden successfully.
- Jake
  - Pass precheck WITHOUT any pre-hardened macros that require power ports
  - Work on getting standard cell/DFF/clock mux to harden with power pins
  - Document hardening efforts
- Will
  - Keep helping to harden the integrated module
    - Get Clock mux to harden
    - Help get custom cell to harden
- Cade
  - Create branch and attempt to help work through hardening issues

Meeting Notes from Previous Week with Dr. Duwe

10/25/23

Updates from us

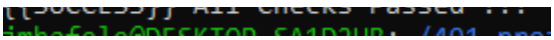
- Saturday Hardening
    - LVS power pin fails during precheck
    - Unable to get DFF, clk mux, or SRAM to harden in user_proj_final
- Make PDKs breaks
    - Error when cloning one of skywater PDKs breaks
    - When does this happen?
    - Do we need those other libraries?
- DFF Custom Cell
    - Cell is complete
    - Did simulate in LTSpice
    - Generated GDS and LEF files
- SRAM
    - Bug in behavioral model of SRAM that fails when hardening due to pin checking
    - Stole newest SRAM from most recent verified test chip
    - Input port was std_logic_vector of length 1, was flattening to bit

Anything not working?

- DFF cant harden
- DFF not possible to sim because we had to add behavioral model
- Standard cells in PDK have Verilog behavioral model

Bi-Weekly Progress

- Gregory
  - Integrated the DFF with caravel, it failed placement. It appears that a 10x by 2x-sized standard cell is too large to be placed. I created a smaller 2x1 NAND gate and it worked perfectly
  - Currently our custom cell is now a NAND gate
  - The DFF might work if we set it as a macro with manual placement coordinates, but automatic placement failed.
- Jake
  - Found new PDK, Openlane, and Caravel Git Commit tags for more recent builds, updated project with new commit tags
    - Use ‘make pdk-with-volare' to build skywater PDKs, NOT ‘make pdk’
  - Got sample project to harden and pass LVS precheck, which was giving us trouble last time
  - Hardened final wrapper module for design to insert and hardened with sample project contents, to verify defining correct files for project_wrapper hardening
  - Got our design modules including SPI, wishbone, and standard cell test to harden and pass precheck
  - Updated user guide to include info on some precheck information and updating git commit tags
- Will
  - Helped pull in updated caravel user project repo to rebase our project on.
  - Hardened user project final with just the behavioral verilog inside of it
  - Was able to harden project wrapper with the user proj final macro inside of it when we are only using the behavioral modules
  - Hardened wrapper was able to pass precheck when we were only using behavioral models
  - Started to harden dsp module with memory
    - Was able to get it to harden when dsp module was set to be the top level module in the design
    - This lead to problems when making the wrapper as there were more than one top level modules instantiated.
    - Found solution that still needs to be implemented but essentially the memory must be instantiated in the wrapper and cannot be a part of a macro.
- Cade
  - Was there for part of Saturday, built pdk without errors but it did not include all necessary libraries.
  - Attempted to rebuild with new pdk that jake found, but still running into same issue



Precheck pass for example project

Individual Contributions

Team Member	Contribution	Hours per report	Total Hours
Jake Hafele	Hardened and ran precheck for example project and behavioral designs	25	160
Gregory Ling	DFF integration, made a new NAND gate instead, and got it to harden in caravel	25	116
Will Galles	Hardened behavioral models. Worked more on hardening memory	25	160
Cade Breeding	Working through hardening issues. Attempting to get to spot of working harden that rest of group is at	15	95

Plans for Upcoming Two Weeks

- Gregory
  - Test DFF manual placement coordinates, help in the final hardening/bring up plan
- Jake
  - Help integrating prehardened macros (custom DFF, SRAM, clk mux)
  - Document hardening efforts and precheck process
  - Discuss next steps AFTER hardening success (more functional testing would be cool)
- Will
  - Rework project to have memory instantiated in the user project wrapper
  - Get the memory to harden by itself in the top level.
  - Get all the previously hardened modules along with the dsp module to harden with the memory.
- Cade
  - Confer with group to discuss solutions from Saturday and discuss next steps