EE/CprE/SE 492 Bi-WEEKLY REPORT 4

Digital ASIC Fabrication

10/11/2023 – 10/25/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breedings

Past Week Assignments

- Gregory
  - Create the D-flip-flop in xschem, magic, and simulate in ngspice
- Jake
  - Assist in integrating top level design modules into Verilog testbench
  - Work on documentation for using simulation/hardening tools (using macros, etc)
  - Start considering C code testing with Verilog wrapper and bringup plan
- Will
  - Write more in depth test cases to test out the DSP module
  - Focus on edge cases that could break it
  - Start adding the module into the top level design
  - Make sure that the communication protocol matches what the rest of submodules
  - Add protection to reject data when the module is not asking for it (think is working but verify)
- Cade
  - Finish and integrate clock gating

Meeting Notes from Previous Week with Dr. Duwe

No meetings with Dr. Duwe, we typically meet every other week and Dr. Duwe was traveling.

Bi-Weekly Progress

- Gregory
    - Custom Cell is complete!!!!!
    - See pictures and notes below
- Jake
    - Integrated individual module designs into user_proj_final and testbench
        - DSP module
        - DFF Custom Cell
        - Standard Cell AND Gate
        - Clock Mux
    - Worked on hardening efforts for SPI, standard cell, DFF cell
    - Worked on hardening efforts for user_project_wrapper
    - Investigated caravel precheck run
- Will
    - Finished off wirting last part of DSP module
    - Got DSP module to harden
    - Helped integrate and harden the rest of the modules
- Cade

XSchem & Magic Notes

XSchem

1) Install from https://xschem.sourceforge.io/stefan/index.html
2) Clone open-pdks and install it
```sh
git clone https://github.com/RTimothyEdwards/open_pdks -b open_pdks-1.0
```

3) Configure
```sh
cd open_pdks
./configure \
--disable-primitive-gf180mcu \
--disable-verification-gf180mcu \
--disable-io-gf180mcu \
--disable-sc-7t5v0-gf180mcu \
--disable-sc-9t5v0-gf180mcu \
--disable-sram-gf180mcu \
--disable-osu-sc-gf180mcu \
--prefix="$(pwd)" \
--enable-sky130-pdk \
--enable-xschem
make
make install
```

The PDK is now available in $(pwd)/share/pdk

4) Copy xschemrc from open_pdks/share/pdk/sky130A/libs.tech/xschem/xschemrc to the directory in which you want to save your xschem project

5) In that same folder, run `PDK_ROOT=$(pwd)/../open_pdks/share/pdk/ xschem &`

6) Keyboard shortcuts:
U = Undo
Shift + U = Redo
Shift + I = Insert
C = Copy
M = Move
W = Wire
Shift + W = Snap Wire

Simulation Data:
https://xschem.sourceforge.io/stefan/xschem_man/graphs.html
https://xschem.sourceforge.io/stefan/xschem_man/tutorial_run_simulation.html

Spice Manual:
https://ngspice.sourceforge.io/docs/ngspice-41-manual.pdf

SKY130 Inverter:
http://web02.gonzaga.edu/faculty/talarico/vlsi/xschemTut.html

Running a simulation:
Generate a netlist by clicking the Netlist button in the upper right corner, or press `n`.
Run the simulation by clicking the Simulate button in the upper right corner, or run ngspice manually.
Load the waveform by holding ctrl and clicking the Load Waves button to load the waves from the .raw file produced by the simulation.
Double-click the graph body to change the nets shown. Digital mode will stack the graphs as separate waveforms instead of overlapping in space.

Magic
Install Magic & openpdk above
- Magic must be installed from source, needs 8.3.411+, APT only has 8.3.108

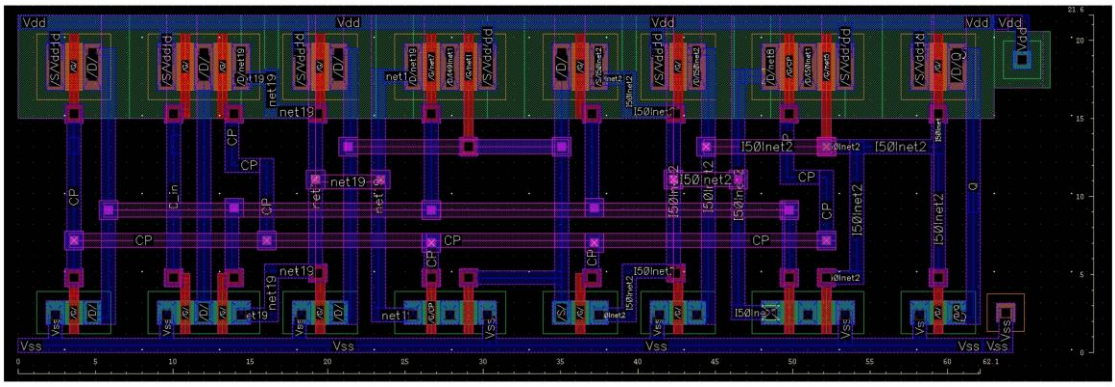
git clone https://github.com/RTimothyEdwards/magic

In your magic workspace,

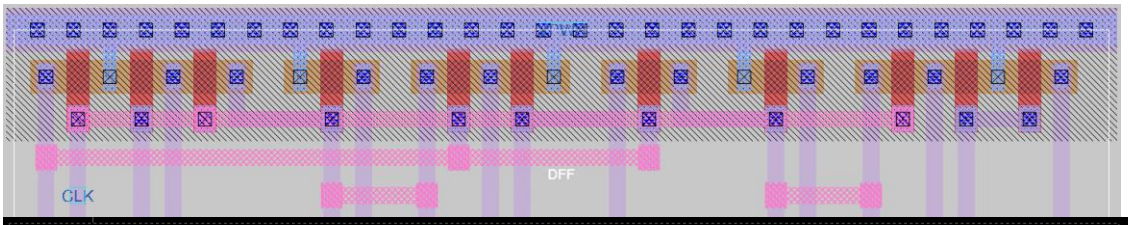
https://isn.ucsd.edu/courses/beng207/lectures/Tim_Edwards_2021_slides.pdf

https://skywater-pdk.readthedocs.io/en/main/rules/periphery.html#npc
https://skywater-pdk.readthedocs.io/en/main/rules/layers.html

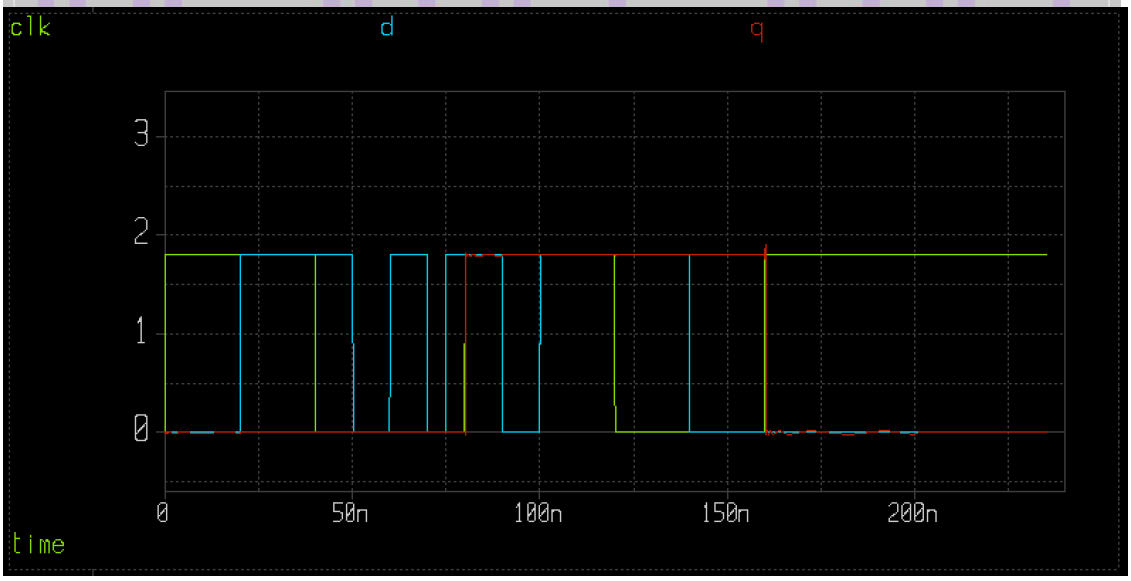
Note: licon = viali



Reference DFF design from EE465 lab

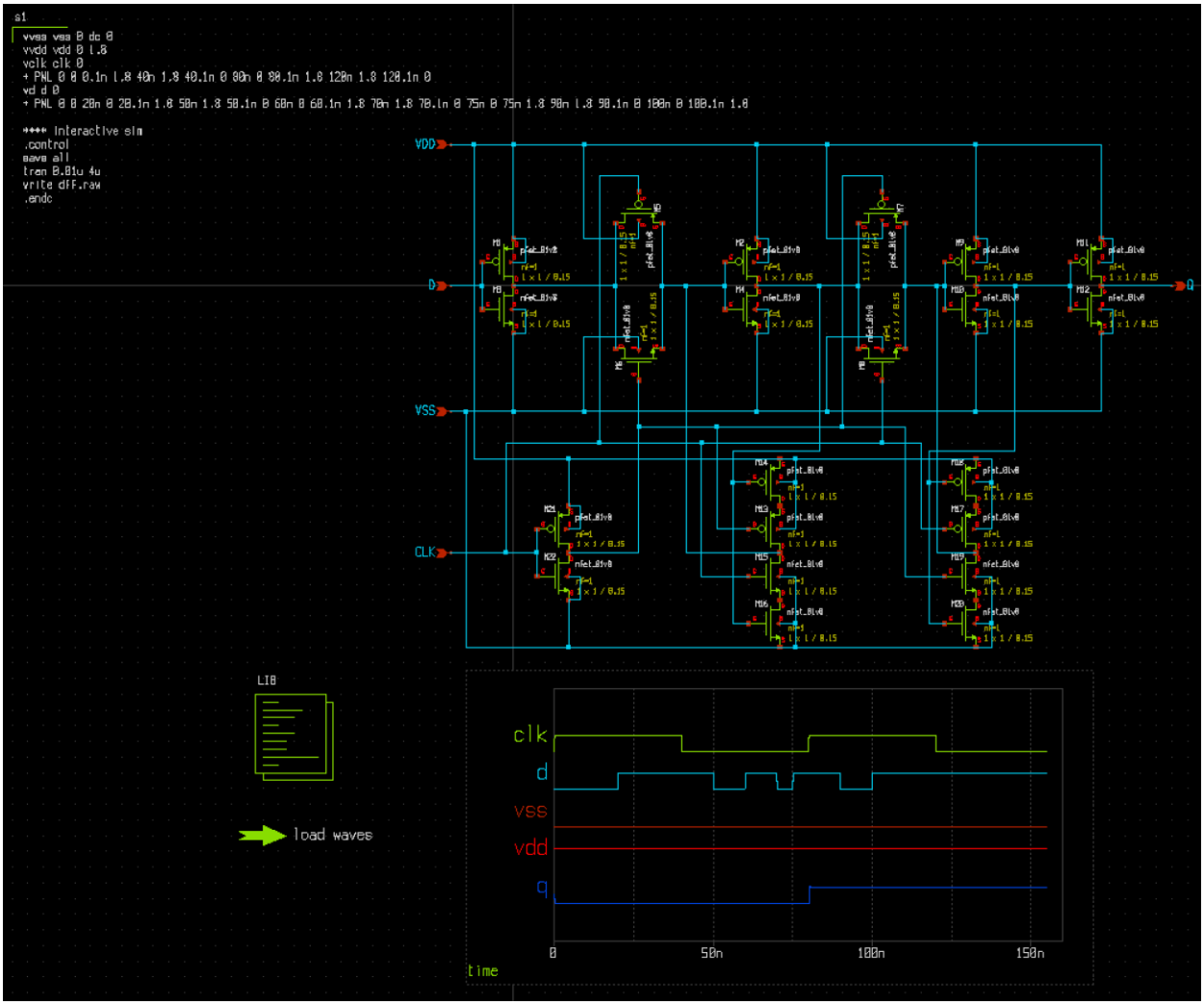


Custom DFF Cell Layout in Magic

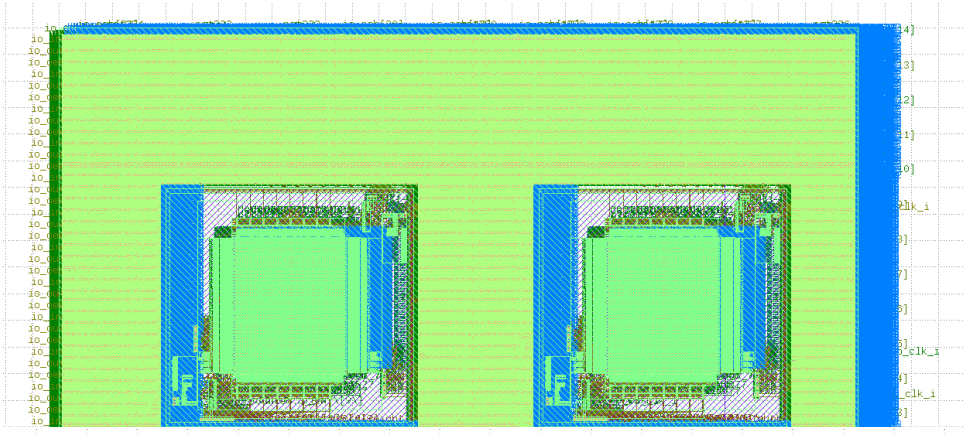


Ngspice

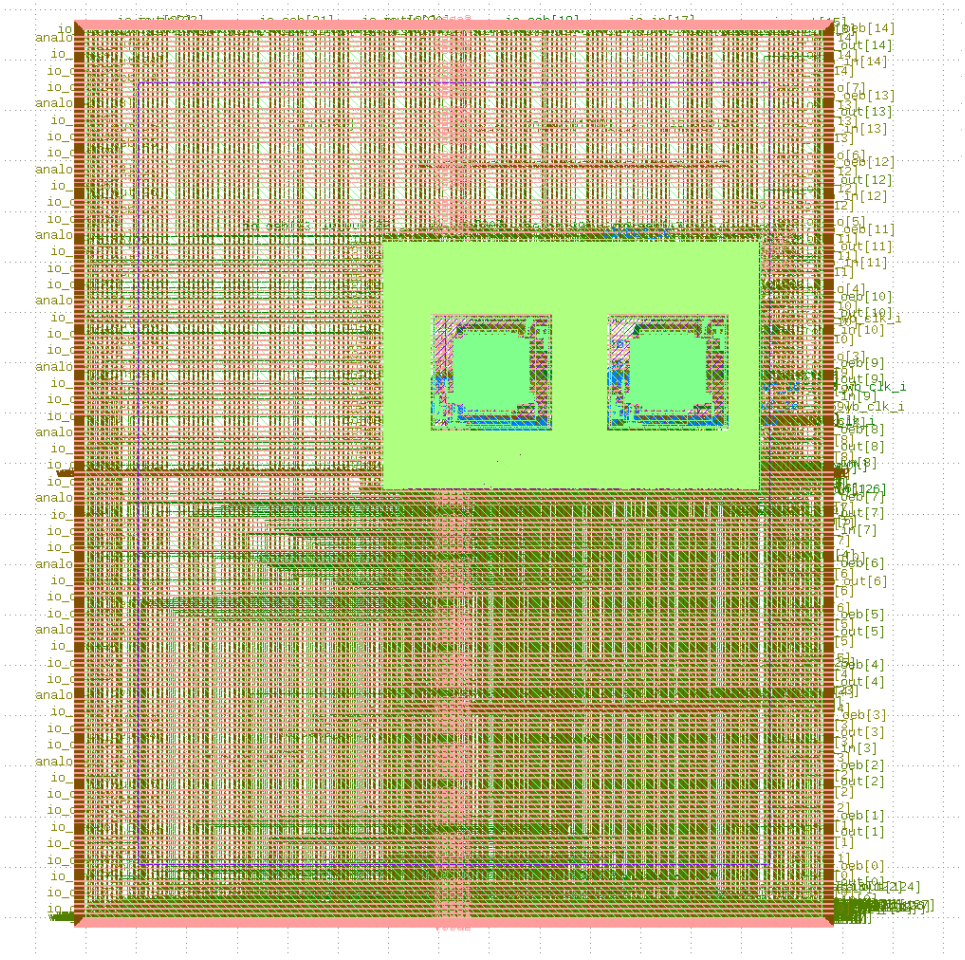
simulation of Magic DFF design



DFF Schematic in XSchem



Top level design with standard cell test, SPI interface, wishbone bus, and DSP module hardened in user_proj_final module



Top level design inserted into the required

user_project_wrapper

Individual Contributions

Team Member	Contribution	Hours per report	Total Hours
Jake Hafele	Top level integration, hardening top level modules, researching precheck	30	135
Gregory Ling	XSchem & Magic DFF design	20	91
Will Galles	DSP module verilog and hardening, assisted whole module hardening	25	135
Cade Breeding	Mostly various debugging	10	80

Plans for Upcoming Two Weeks

- Gregory
  - Import the custom DFF into the wrapper and get it to harden successfully.
- Jake
  - Pass precheck WITHOUT any pre-hardened macros that require power ports
  - Work on getting standard cell/DFF/clock mux to harden with power pins
  - Document hardening efforts
- Will
  - Keep helping to harden the integrated module
    - Get Clock mux to harden
    - Help get custom cell to harden
- Cade
  - Create branch and attempt to help work through hardening issues