EE/CprE/SE 492 Bi-WEEKLY REPORT 3

Digital ASIC Fabrication

9/28/2023 – 10/10/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breedings

Past Week Assignments

- Start making the a D flip flop for the custom cell that we are implementing
- Clean up master branch to prevent simulation failures
- Create top level test bench for the final top level module
- Finish the subcomponents of the DSP module
- Connect all the subcomponents together in a top level module to finish the DSP module
- Finish writing test case and hardening module

Meeting Notes from Previous Week with Dr. Duwe

9/27/23

Updates from us

- Will
  - counter submodule tested with the testbench
  - Memory unit tested with testbench
  - Need to write MAC unit
    - Use an adder tree or reduction tree
    - Limited by number of read ports on the memory, so at best two mac units
    - Duwe disagrees -> How much can you read from a port? 8 or 32 bits?
    - Nope. It's 8 bits, otherwise you could read wide and perform SIMD
    - Multiple memory modules? You could probably put more than two, one for weights and one for data. And have more MAC units as a result. That's a space issue at the end.
- Gregory
  - Magic works, I got the example inverter working
  - LEF and spice netlist exported, need to try simulating in spice
- Cade
  - Modules done in Verilog
  - Testbenches work for standard cell module
  - Finishing testbench for clock gating module
  - Be careful of hold time violations with the clock gating module
  - Be sure to run static analysis on it to ensure timing works
- Jake
  - Overall massive testbench to test integration of all modules in progress

TODO

- Start looking into the bring up plan
  - Get a nucleo board?
  - Show that we have the wrapper scripts running
- Need to work with Jake on integrating with Jake's framework
- Gregory working on the D-flip-flop in Magic

10/4/23

- Updates from us
  - Gregory
    - "I discovered the way I was using magic was completely wrong"
    - Need to use actual tech lib from skywater pdk
      - Has makefile to generate tech file
    - Talk to analog team in senior design
      - Talk to Josh
      - Can also ask on slack

        - Using xschem for schematic capture, spice for simulations
        - Should be no DRC errors/warnings
    - Jake
        - Integrated gregorys wishbone bus into top level module for user area
        - For user guide, highlight unique aspects that you added
            - For 492, submit everything together
            - As deliverable for dr. Duwe, keep everything in one place
            - Black boxing, hardening, simm
    - Will
        - Got MAC unit to work with loading sample weights
        - Can use existing wishbone/spi busses for read/write transactions
        - How to load random data?
            - Use verilog tasks
            - Load data from text file
        - Add more processing elements/memory
            - Same ports top level
    - Cade
        - Still working on clock gating
        - Static timing analysis
        - Start with simple test of clock gating and simple modules
            - Make sure it can get through signoff
        - STA is provided
            - Run SDF gate level simulations

- General
    - Timeline
        - Functional designs done in middle October
        - All modules together at end of October
        - Use November for bringup plan/design document
    - Design Document additions?
        - Add testing results and appendix
    - Other deliverables
        - User Guide
            - Add complete one document guide for using toolflow, hardening, simulations, magic, etc
        -

- TODO
    - Create total user guide on using toolflow
        - Hardening, running sims, magic
    - Use smaller C files for verification, intent for bringup plan
    - Work on functional designs/simulations

Bi-Weekly Progress

- Gregory
  - CMOS inverter complete in Magic. Can't simulate because it used the wrong PDK
  - Got correct PDK installed with xschem, started schematic layout of d-flip-flop. XSchem seems to have quite a few interesting things in here.
  - 
- Jake
  - Created top level testbench for design module wrapper
  - Integrated SPI and Wishbone read/write tasks to top level testbench
  - Included wishbone test in top level wrapper testbench to verify SPI and wishbone read/write transactions with Gregorys counter test
  - Created spreadsheets to map out all I/O and Logic Analyzer input and output ports for the chip and microcontroller
- Will
  - Got mac unit created and tested separately
  - Created Top level DSP module that would connect the memories, counters, and the mac unit.
  - Tested the three basic states that the module can be in
    - Loading weights
    - Preloading data
    - Loading in single data and preforming convolution
  - Have basic test benches that can test each stage with simple data.
  - Creating framework for more complicated data tests
- Cade
  - Fixed Standard Cell test to be not use la pin so that it can be used in top level
  - Looked into how to do timing analysis for clock gating

Individual Contributions

Team Member	Contribution	Hours per report	Total Hours
Jake Hafele	More top level testbenches, integration efforts	15	105
Gregory Ling	CMOS inverter, Magic, and XSchem setup.	10	71
Will Galles	Finished basic DSP unit and all submodules inside	20	110
Cade Breeding	Modified Standard Cell and Testing for Clock Gating	10	70

Plans for Upcoming Two Weeks

- Gregory
  - Create the D-flip-flop in xschem, magic, and simulate in ngspice
- Jake
  - Assist in integrating top level design modules into Verilog testbench
  - Work on documentation for using simulation/hardening tools (using macros, etc)
  - Start considering C code testing with Verilog wrapper and bringup plan
- Will
  - Write more in depth test cases to test out the DSP module
  - Focus on edge cases that could break it
  - Start adding the module into the top level design
  - Make sure that the communication protocol matches what the rest of submodules
  - Add protection to reject data when the module is not asking for it (think is working but verify)
- Cade
  - Finish and integrate clock gating