EE/CprE/SE 492 Bi-WEEKLY REPORT 1

Digital ASIC Fabrication

8/21/2023 – 9/10/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breedings

Past Week Assignments

- Meet for first time of semester with Duwe
- Set weekly meeting times with advisor (Duwe)
- Complete SPI verilog and testbenches
- Complete wishbone test
- Get started on other design modules

Meeting Notes from Previous Week with Dr. Duwe

8/21/23

We are BACK!!

TODO:

1. Find a meeting time for this semester
2. Make sure we are working in the first few weeks before other classes murder us

Meeting Time

- More critical to meet weekly in 491
- Will block out time for weekly meetings, and we can decide if we want to attend

ChatGPT Digital ASIC

MPWShuttle Deadline

- No internal deadline

- Anything that would come back would be at end of semester
- Reported previous project back in November as of today

Goals
- Early in semester complete digital design
- Spend later part of semester on bring up plan for our design
    - Write python script to interface
    - USB to SPI
- Think about bring up for incoming chip

9/6/23

Updates from us
- Wishbone Bus
    - Gregory got RTL design and testbench run
    - Jake hardened comm control bus for wishbone/SPI interfaces
- Comm Control
    - Gregory designed RTL
    - Jake tested with backdoor SPI testbenches
    - Same architecture for SPI and wishbone bus
- Backdoor SPI
    - Got RTL simulations done for backdoor SPI
    - Coming into roadblocks
- Custom Cell Test
    - Gregory got magic installed
- Hardening
    - Will figured out how to get different user modules hardened inside top level user area wrapper
    - Harden all different modules and route together in top wrapper
    - Reference as VERILOG_FILE_BLACKBOX and include REF and GDL files
    - Is it worth it to make hardened black boxes or throw all in top level?
    - For all together:
    - May take very long
    - Tools may not be powerful enough
    - Would save space
    - Separate black boxes
    - Will save time
    - Lower risk (?)

Notes
- In final design may not want Logic analyzer fully hooked up, lots of overhead
- Can we use a hardened netlist for signoff?
    - Get SPEF or SDF files from hardening
    - What power signoff tools can be used?
- MPW7 has still not been sent to packaging
- Add a CI/CD when pushing design

TODO

- Gregory work on custom cell in Magic
  - "I have no idea where this is going to go"
- First biweekly report due next week
- Presentation in lecture next week
- Update Gantt chart to track progress of each module
- Get more experience hardening modules
- Request VM in Dr. Duwes name as owner for hardening
- Add Duwe to Git repo

Bi-Weekly Progress

- Gregory
  - Wishbone bus RTL & Testbench written
  - Comm control RTL & Testbench written
  - Magic installed and new project created for custom cell design
- Jake
  - Finished top level backdoor_spi implementation and testbench
  - Tested backdoor_spi with module_control interface to decode/MUX data from design modules to master SPI
  - Setup config files for hardening spi module, debugged synthesize errors
  - Included documentation updates for spi design modules in submodule design folder
- Will
  - Figured out how to harden both individual modules and combine them in the total project wrapper
  - Started to setup OpenRAM environment to add in memory to user area.
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- Cade
  - Getting back into the project, minor updates to my modules

Individual Contributions

Team Member	Contribution	Hours per report	Total Hours
Jake Hafele	SPI design/testing, hardening	15	75
Gregory Ling	Wishbone bus, Comm control, Magic setup	15	61
Will Galles	Hardening, OpenRAM	15	75
Cade Breeding	Minor updates	3	48

Plans for Upcoming Two Weeks

- Gregory
    - Design something in Magic
    - Try to schedule a meeting with Maruf Ahamed or Alex Stoytchev to ask about the Magic layout.
    - See about importing a Magic project into Cadence for simulation (Ask Jake)
- Jake
    - Integrate hardened designs of backdoor_spi and control_module interfaces
    - Push validated spi design to main
    - Setup config files and SPI integration in main branch of git
    - Create excel spreadsheet to decode data for wishbone/spi for every module
- Will
    - Finish setting up the openRAM environment.
    - Implement a memory bank in the user area.
    - Harden the memory bank.
    - Put together a small test bench to ensure the memory's functionality.
- Cade
    - Push changes and finish standard cell module