EE/CprE/SE 491 WEEKLY REPORT 9

Digital ASIC Fabrication

4/11/2023 – 4/17/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

- Gregory – Finish wishbone test
- Jake – Get shift register test fully functional, expand to shift out and backdoor SPI module if successful
- Will – Figure out the ratio of memory to multipliers that we are able to implement for the
- Cade – Write the standard cell test in Verilog

Meeting Notes from Previous Week with Dr. Duwe

4/10/23

- Updates from us:
  - Test plan assignment
    -
  - Lightning talk
    - Overall feedback was pretty good
    - Some were unsure about the goal and why we were doing it
    - Highlight top level design and purpose more for end of semester presentation?
  - Will learned about memory
    - 8 bit vs 12 bit? Not yet covered
    - What was found for RAM?
      - Found documentation open the generator openRAM

        - Found another project from two years ago where a 4 kB block was implemented
        - SUPOSSEDLY a 1 kB block is silicon proven
        - Ask previous team that is currently trying to use RAM
    - Jake SPI testing
        - Run robust tests outside caravel module in verilog testbench
            - Allows us to find edge cases better for each individual module
        - Run top level integration with C code to try some edge cases after everything is pushed together
            - These take MUCH longer
            - This will be useful later
        - Clock domain crossing?
            - We could use the same SPI process of command, address, data that housekeeping SPI module uses
    - Gregorys wishbone test
        - Working on writing state machine in Verilog
        - Using 'always *' will enter when any included signals change
- Panel presentation
    - Want best feedback we can
    - To do this, make presentation as clear as possible
    - Have backup slides and more detail ready
    - Panel assigns 25% of grade
    - High variability among the panel
    - Next week or following we should have general draft
    - Week 14 should give practice presentation
    - Give practice monday morning of dead week
    - How to cast things
        - Articulate project scope, users, why ours is a little odd
        - Don’t want to present anything we are not willing to defend, or atleast give a nuanced reason
        - KNOW YOUR ACRONYMS, including SPI or FFT for example
        - If we don't know, admit it because xyz instead of 5 minute distraction
        - Defend your argument, but DO NOT be defensive
        - Be thankful for feedback
        - Have backup slides showing preliminary tests, modular designs, etc
        - Try to understand the question/concern and try to answer them. They may be the same as ours for the project
        - MUST MUST MUST MUST MUST MUST HAVE THE DESIGN DOCUMENT AND THE PRESENTATION ON OUR WEBSITE BEFORE PRESENTING

TODO:

- Jake - Do writeup for clock synchronization for backdoor SPI
- Jake – Work on SPI testbenches OUTSIDE of caravel module
- Start on panel presentation draft

Weekly Progress

- Gregory – More progress on wishbone test
- Jake – Successfully tested shift in and shift out registers for SPI module WITHOUT wrapped in caravel module
- Will – Worked on the component diagram for the DSP module shown below
- Cade – No new updates

Jake found a bug: If a C file is not present in the /verilog/dv testbench folder, the makefile will generate an error since there will be NO hex file made. This hex file is not used UNLESS you are instantiating your module under the top-level caravel module and wrapper. Either way, the C file needs to be present to run RTL simulations so that the makefile can generate a waveform output for GTKWave

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Created shift out testbench, verified shift in and shift out modules	8	48
Gregory Ling	More slow progress on the wishbone test	3	36
Will Galles	Designing the architecture of the DSP module	5	50
Cade Breeding	Some continued work on the standard cell module	1	35

Plans for Upcoming Week

- All – Work on finishing design document and creating the presentation
- Jake – Harden and run gate level simulation for shift in/shift out registers

Component Diagram of the DSP module