EE/CprE/SE 491 WEEKLY REPORT 8

Digital ASIC Fabrication

4/3/2023 – 4/10/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

- Will – Finalize the design schematic for the Voice Road Noise Isolation
- Jake – Begin writing the SPI module in Verilog
- Gregory – Try working through the custom cell instructions
- Cade – Write the standard cell test in Verilog

Meeting Notes from Previous Week with Dr. Duwe

3/27/23

Updates from us:

- Completed the design plan and lightning talk
  - Creating an ASIC is not cheap to develop mask
  - Included design specification as appendix
  - Included system diagram we worked on
- Will learned about memory
  - FFT would need lots of memory
  - Compared to direct convolution in time domain
  - Orders of magnitude of more memory needed for FFT version
  - Could we do direct convolution and shift through input?

        - 1024 samples (one bank of RAM)
        - Each sample is 12 bits
    - How many multipliers can we fit/cycles to break down for different chunks?
    - Quality indicator? Can we go from 12 bits to 8 bits for sample?
        - Perceptual evaluation of speech quality
    - Is RAM or shift register better?
        - In terms of energy ram is better
        - Not reading ALL of ram in one cycle
        - Could get one 1 kB banks or 2 512 Byte banks
        - Preload first time and fill pipeline,
    - Convolution comes down to 1 timed value
    - Look into OpenRAM
- Backdoor SPI module
    - Do we need to define skywater cells specifically in submodules? No, synthesis handles it
        - Elaboration from behavioral into interpretation
    - Wrote verilog code for shift registers
    - Got stuck on example simulation, deleted a newline accidentally
    - Should be able to get gate level netlists with openlane hardening

Weekly Progress

- Gregory – Started writing verilog for the wishbone test
- Jake – Developed verilog and C code testbench for the shift in register. Created a new user wrapper to run the RTL simulation
- Will – Started to put together in depth component diagram for the DSP module

Pending Issues

- Jake – I followed the sample code given for the two logic analyzer tests, which drove a clock and same control/data signals through the logic analyzer probes for a counter. When creating my own code, I noticed it took a VERY long time for the simulations to run because the code would update the data signals and clock in the ms range. Could I reduce the timestep for the testbench to help with this? Should I test these modules directly without the logic analyzer or GPIO interface directly?

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Developed Verilog and C code for shift in register test. Still debugging rtl sim	6	40

Gregory Ling	Testing Plan, started verilog for wishbone test	3	33
Will Galles	Testing Plan, started the in-depth component diagram for the DSP module	3	45
Cade Breeding	Working on standard cell test	4	34

Plans for Upcoming Week

- Gregory – Finish wishbone test
- Jake – Get shift register test fully functional, expand to shift out and backdoor SPI module if successful
- Will – Figure out the ratio of memory to multipliers that we are able to implement for the