EE/CprE/SE 491 WEEKLY REPORT 6B

Digital ASIC Fabrication

3/3/2023 – 3/26/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Draw out specifications for each module with enough detail for us to verify integration is likely to work and ensure each member has a clear goal in mind for implementation in the next few weeks.

Meeting Notes from Previous Week with Dr. Duwe

3/20/23

Updates from us:

- Created a design specification document to define each module
  - Includes backdoor SPI, DSP module, Clock Gate, Standard cell test, custom cell test, wishbone test

Discussion:

- Clock gate module
  - Clock gating entire user area (run off clocks produced here)
  - Can turn on and off each piece individually
  - Can control clocks individually for DSP, wishbone test, and external clock

        - Assume SPI will always be on
    - Road noise isolation
        - How does it fit within whole design?
        - Where does data come to and from?
        - Was too slow on MCU, Isaac was looking towards FPGA
    - Standard cell test
        - One of easier modules
        - Able to test different standard cell libraries
        - Good for risk mitigation
    - Custom Cell Test
        - More complex hardware than standard cell
        - Define behavior of cell in Verilog
        - Use magic in OpenRoad to define cell?
        - Black box in Verilog for design
        - Define blackbox either behaviorally or with primitive for sim?
    - Design Document
        - ALWAYS more room for technical documents in the appendix
        - Reference in design document from Appendix
        - Also include details test plans in appendices
            - Should be able to hand some part of design document to a 288 student that would be able to test our chip
            - Should not be open for interpretation
            - Heres the module, expected behavior, how it fits in to total design, and then satisfies the requirements
    - Bank explosion
        - Silicon Valley Bank went under
        - Bailout from government, possible risk to delaying MPW delivery?
        - Good to include as real world risk
        - Actual deliverable is GitHub artifact that passes the precheck conditions
        - Will be able to deliver technical design that passes requirements
    - Timelines
        - Gantt chart recommended
        - Estimate timeline relative to module complexity
        - Standard cell design is low time variability
            - Wishbone also
        - Custom cell design is not a lot of work, but it is new
            - Multiply factor by at least 6 of what it takes, to at least 12
            - Work through more bugs in the process, ask on slack, etc
        - SPI
            - Relatively shorter design wise
            - Have to deal with I/O, slightly more complex
            - Medium time
        - Road noise
            - Even at design level, issues like fixed point vs floating point
            - Develop test plan, design such that algorithm done in fixed point, able to compare to implementation
            - Before settling in design, able to know it works

        - Gap too big from floating point and fixed point, think of software implementation of fixed point
        - Higher planning time
    - Consider starting integration earlier than being completely done
        - Could be more practical, does it need to be on Gant chart
        - Preliminary design to integrate
        - Issues for hardening came in when design approached a large fraction of user area
        - 5-10 adders, hardening became challenging by tweaking parameters
        - Suggestion with temporary design with most of components are in, try to integrate fully
        - Could sub in standard cell size for the custom cell version
            - Helps with integration hardening before bugs worked out in modules
        - Can kick one module off if scope becomes too large, so we get back a chip still
            - Probability of success does not stack on each module together, treat as isolated pieces that can act separately
    - Moderately track time spent for each module
        - Make as accurate as we can

TODO:

- Create a top level module decomposition
    - Powerpoint
- Set up a meeting with ISU alumni Isaac Rex to go over proposed DSP algorithm
    - Analog to digital conversion with transceiver?
    - How did he deal with car environment?
    - What was he doing with voice audio? Cant it go through MCU or I/O pins
- Start writing tests and Verilog modules for each subcomponent
    - Make MUCH more step by step than a lab manual

Weekly Progress

- Got the details for implementing the DSP module and how the whole system works
- Created Design spcification file that describes all of the modules that we plan to implement
- Finalize functionality of the Backdoor SPI functionality

Pending Issues

- N/A

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Research inout port and I2C module	3	28
Gregory Ling	Write detailed specifications	3	28
Will Galles	Investigate DSP project	9	37
Cade Breeding	Course Paperwork	3	28

Plans for Upcoming Week

- Draw out the overall architecture of the design and begin writing verilog