EE/CprE/SE 491 WEEKLY REPORT 6

Digital ASIC Fabrication

3/5/2023 – 3/12/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Post skywater custom cell documentation in general eFabless chat in this teams channel
- Define what we are implementing to test clock gate
    - Experimenting right now, get solidified test plan running
- Solidify overall design specced out
    - What all do we want? Subject to change, get some ideas churning
    - I2C communication, wishbone test
    - How to design control configuration
        - As much redundancies as possible
    - Find a lead for each subcomponent

Meeting Notes from Previous Week with Dr. Duwe

3/6/23

Updates from us:

- Will was working on getting the clock gate cell and clock mux component into a testbench
    - Rebuilt the entire caravel wrapper framework around it
    - Clock gates work well in simulation
    - When adding clock MUX, it could not find the module
    - Gregory found that most components in the management wrapper are in high density library, and the clock mux was in the low leakage library.

        - Is only high density imported?
    - Clock MUX can switch between two different clocks
        - One side is the default clock for redundancy if clock gate fails
        - Other side is output of gated clock module
    - From Duwe:
        - Consider having digital logic components reset through logic analyzer pin
        - Would be able to reset from the wrapper
        - Switch config via the wrapper MCU, something is in weird state
        - If in some unintended state, design so able to get out of that state
    - Glitching when on/off handled in clock gate cell
        - Synchronize clock signals
        - Cross coupled D flip flops
- Found instructions how to create own cell with skywater documentation
    - Useful if we need to do physical layout ourselves
    - Could we make our own test component?
- Paperwork
    - Worked on project description and requirements
        - Don't need to specify functional and nonfunctional requirements
        - Did have to specify quantitative constraints
        - From Duwe:
            - Start with OUR requirements from project description, then add efabless and skywater requirements
            - EFabless requirements more like constraints
            - Think of how you are mentally reading the design document
            - Requirement: A goal we must achieve
                - Operate at 50 MHz or above
                - Did you meet the requirement? YES or NO
                - Functional requirement: does it output X test string with testbench?
            - Constraint: something that is imposed upon us by the environment
                - Hooking up test bench to certain probes, based on ENVIORNMENT
                - We have access to eFabless, we are limited to their toolflow and libraries
                    - Constraint is that we HAVE to use this process
                    - This constraint has following requirements to USE those tools
            - Standards:
                - Is the Skywater 130 nm process a standard?
                    - Search for a document
                - Perform a requirement in the bounds of the constraints
                - UART has a standard with RS232
                - SPI/I2C should have standard document numbers
    - Reports under the Files/Reports module
    - Design Document sections under Files/Design Document
- Previous teams paperwork

        - We saw a gant chart was built. Should we do this?
            - Duwe: We should develop a gant chart
                - Speculate next MPW due date
    - Can we use the Gitlab repo for OpenMPW submission?
        - May not be open for them to view

TODO:

- Post skywater custom cell documentation in general eFabless chat in this teams channel
- Define what we are implementing to test clock gate
    - Experimenting right now, get solidified test plan running
- Verify if lab report due over break (March 12/19?)
- Solidify overall design specced out
    - What all do we want? Subject to change, get some ideas churning
    - I2C communication, wishbone test
    - How to design control configuration
        - As much redundancies as possible
    - Find a lead for each subcomponent
- Find Dr. Duwe a mouse

Weekly Progress

- Start to design component modules and interface between
- Made more progress with clock
- Posted skywater custom cell documentation in general eFabless chat in this teams channel

Pending Issues

- N/A

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Research inout port and I2C module	3	28
Gregory Ling		3	28
Will Galles	Continue to develop clock test module	3	28
Cade Breeding		3	28

Plans for Upcoming Week

- Expand clock test
- Continue to define components and interfaces
- SPRING BREAK!! 😊