EE/CprE/SE 491 WEEKLY REPORT 5

Digital ASIC Fabrication

2/27/2023 – 3/4/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Look at standard cell library
    - What sets of cells exist that we can use?
    - Use for power/clock gating
    - Do such cells exist? Give a reference and research
    - Sddec23-08 analog team may be able to point us in right spot
    - https://skywater-pdk.readthedocs.io/en/main/contents/libraries/foundry-provided.html
    - UPF – Unified Power Format. Able to define power domains
        - OpenLane support?
- Test clock gating and clock MUX

Meeting Notes from Previous Week with Dr. Duwe

2/27/23

Updates from us:

- Standard Cell Library
    - Skywater documentation was not filled in properly
    - Gregory found a fresh build of the sky water documentation that had more cells listed, some still blank

        - Some cells would just list a name, but we could search for it in the Github Library
        - All cells are there, just not compiled in the documentation
        - Tried Using a standard cell
        - C level simulation took a long amount of time
            - Program running on the microcontroller
            - Verilator should be more performant
            - Emulated entire project wrapper, which took lots of time
            - Did compile and was happy
        - Found parts for clock gating parts
            - Clock gating cell and 2:1 clock mux
        - Didn't find anything on power gating
            - Gregory found one diagram with all power on chip
            - 1.8V and 3.3V power level on user side and management side, independent of each other
            - Routed to each side, no power gating currently
            - There is a high voltage library not listed on the sky water documentation, includes 5V cells
    - Asked last semesters team if they had the original design teams documentation
        - Where would this be?
        - Motive was to solve simpler questions we had
        - Look on their senior design website (sddec22-17)
        - http://sddec22-17.sd.ece.iastate.edu/

Gating Investigation

- What are we looking for in power gating?
    - Memory mapped register to shut off given components
    - How do you shut off power to certain submodules?
    - Sleep input means A will no longer be driving X
    - Normally would hook up Vdd to output
    - If X turns off, no longer powering it but current would leak to X
    - We are looking for header or footer FETs
- Could use a level shifter to cross domains
    - High density, low level leakage
    - https://antmicro-skywater-pdk-docs.readthedocs.io/en/test-submodules-in-rtd/contents/libraries/sky130_fd_sc_hd/cells/lpflow_lsbuf_lh_hl_isowell_tap/README.html
- There is enable pins from the GPIO of the Management SOC externally to 3.3V and 1.8V regulators
    - https://caravel-harness.readthedocs.io/en/latest/supplementary-figures.html#power-domain-splits
- May need to stick to clock gating now
- Could wire half to 3.3V and half to 1.8V regulators and control them globally
    - Could even wire in a switch
- All components in libraries ship with a testbench
- Clock Domain UPF equivalent

- Designing Chip > ASIC Club
- MPW7 status?
    - MPW6 is shipping in May
    - MPW3 shipped month earlier than status
- Know what you want to say two weeks before design review
    - Week 13 what is status of project, nonspeculative
    - Monday Week 14 have a presentation ready
    - Week 15 presentation given

Weekly Progress

- We determined how to specify different power domains in structural Verilog. We have two 3.3V power inputs and two 1.8V power inputs we can use in our design.
- We discovered some documentation which indicates we can make custom cells instead of only those in the standard library
- We verified that instantiating the standard library works as expected by instantiating a multiplexer from the standard library
- There is an issue with the high-density low-level library and those cells do not appear to exist, as the hdll clock mux does cannot be found by the tools when simulating

Pending Issues

- How to split up power sources between 3.3V and 1.8V in behavioral Verilog?
- Start prototyping other design modules
- Can we create a custom cell for use in our design?

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Research inout ports for I2C management	5	25
Gregory Ling	Created a standard cell test	5	25
Will Galles	Tested using a clock gate cell	5	25
Cade Breeding	Research into the use and testing of the wishbone bus	5	25

Plans for Upcoming Week

- Expand clock test
- Start prototyping other design modules in parallel
- Get more comfortable with the caravel wrapper and test framework

Meeting Questions For Dr. Duwe on Monday

- We included you under the role of an advisor/client for the requirements section, does this line up with what we have discussed so far?
- Ensure the requirements from the last class assignment matches his expectations:

Advisor/Client (Dr. Duwe) Requirements

- Test the limits of the eFabless process to the best of our ability including, but not limited to:
    - Test clock gating
    - Instantiating several standard cells provided by eFabless
    - Explore custom logic cells
    - Ensure our design is modular
    - Using the wishbone bus provided in the wrapper project
- Include a bring up plan for future team to test manufactured design once returned
- Test and verify functionality of previous team's manufactured design if it is shipped within a reasonable period of time
- Use the mpw_precheck tool at https://github.com/efabless/mpw_precheck to check our design requirements before submission