EE/CprE/SE 491 WEEKLY REPORT 4

Digital ASIC Fabrication

2/19/2023 – 2/26/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Investigate open cell library from Skywater
- Take a look into power gating and how these cells are used
- Push/Pull from shared Senior Design GitLab Repository

Meeting Notes from Previous Week with Dr. Duwe

2/20/23

Updates from us:

- Want to use compartmentalized modules and space to make 4 or 5 smaller projects
- Included projects:
  - Power gating/clock gating to turn modules on and off
  - Hardware based ALU to hand off to microcontroller
  - Small DSP filter (road noise filter, HDMI)
  - Measure gate delay of caravel process
  - Wishbone test read/write
  - Outside I2C line to run to each component to interface with external µC's
- Added a second adder from the old teams Verilog
  - Set constants to add and subtract and verify waves with simulation
  - No wishbone bus changed

        - Two adders running concurrently

Opinion from Dr. Duwe on project proposal

- Be careful with how to cast it so it doesn't seem too excessive
- Lots of risk mitigation and isolation
- Certain pieces are going to be default accessed through GPIO directly
- Others may be accessed via the wishbone by default
- Default power configuration
- Great proof of strategy for design review
    - First isolate modules and in default configuration, keep independent
    - Able to reference past issues had
    - ALU or wishbone check should be more simple, but less risky to spin up
    - Clock gating or DSP may be more risky, but would have something to fall back on with other modules
- SOL if clock gating dies in default state
    - How to work around this?
- Isolating components may lead to more fragility
- "Seems to work for me" - Dr Duwe
- Concerned about top level modules like HDMI scaler or audio filter
    - May be seen as a stretch goal
- Project in general is incremental
    - Structure work to reflect this
    - Before spending lots of time getting HDMI scaler to work, make sure we understand power gating and isolation down solid
    - Work from the point of a submittable design, and can keep moving between submittable states
- As a group the priority has to be getting the overall system org working
    - If this isn't working, we cant submit anything
- If we got the adder and wishbone working, we could do the summer submission and then add extra modules for the later MPW shuttle deadline
    - No cost to submit, can build iteratively

FRAM

- TI requires extra few processes on top of normal CMOS fab
- Scope back to modularized design more realistic
- **Not going to work because eFabless does not support the extra process required.**
- RIP

TODO:

- Setup project in git and .gitignore
- Begin writing modules!
    - ALU

        - I2C
        - Wishbone test
    - Look at standard cell library
        - What sets of cells exist that we can use?
        - Use for power/clock gating
        - Do such cells exist? Give a reference and research
        - Sddec23-08 analog team may be able to point us in right spot
        - https://skywater-pdk.readthedocs.io/en/main/contents/libraries/foundry-provided.html
        - UPF – Unified Power Format. Able to define power domains
            - OpenLane support?

Weekly Progress

- Decided on a modularized project full of different digital design modules with Dr. Duwe
- Found cells in the standard cell library for a gated clock, 2:1 Clock Multiplexers, and standard 4:1 and 2:1 Multiplexers
    - https://antmicro-skywater-pdk-docs.readthedocs.io/en/test-submodules-in-rtd/contents.html
- Pushed/pulled the sample adder projects in Github between team members. Verified pull from shared GitLab
- Determined some design using FRAM would not be feasible due to complicated fabrication progress

Pending Issues

- The documentation for the Skywater PDK is not fully built and missing lots of information
- Need to fix issues with the gate-level simulation

Individual Contributions

- All contributions were for the group this week.

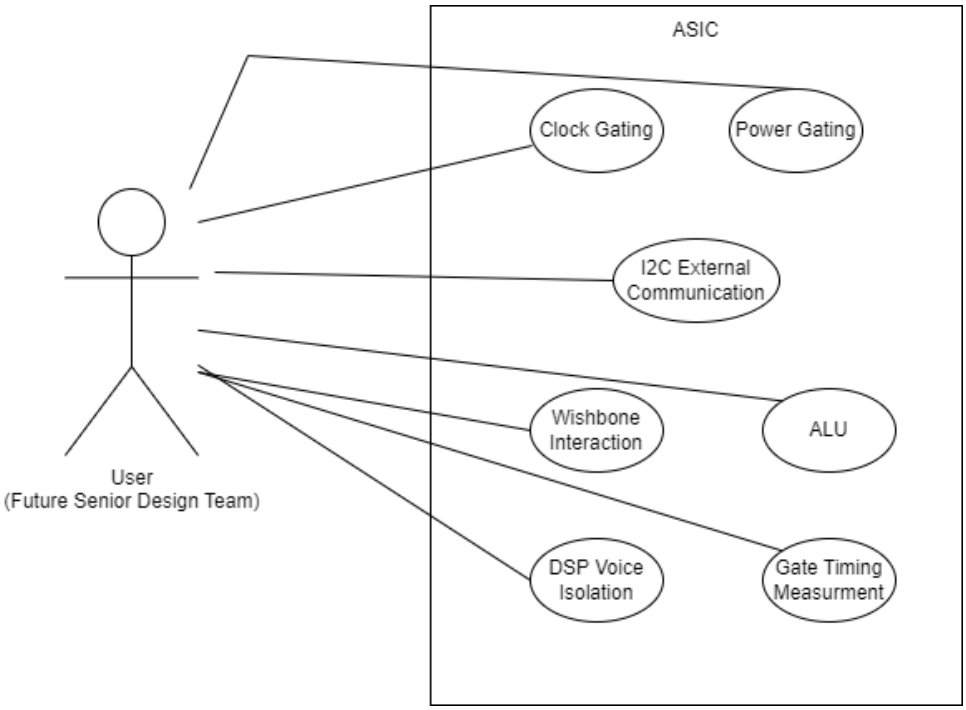
Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Skywater PDK research	5	20
Gregory Ling	Skywater PDK research	5	20
Will Galles	Skywater PDK research	5	20

Cade Breeding	Skywater PDK research	5	20

Plans for Upcoming Week

- Write RTL and testbench for gated clock and clock MUX
- Make some branches in GitLab for individual testing
- Start Wishbone RTL and Testbench code

Use Case Diagram



Meeting Questions For Dr. Duwe on Monday

- How much can we trust the sizing of the standard cells?
- Where can we access the original design team's documentation? Does it have anything on using the standard cell library or integrating these with other modules?