EE/CprE/SE 491 WEEKLY REPORT 3

Digital ASIC Fabrication

2/13/2023 - 2/19/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Test a gate-level simulation
- Modify the basic adder project

Meeting Notes from Previous Week with Dr. Duwe

2/13/23

Updates from us:

- o Met with team finishing their project this semester
- o Got their adder test project in caravel to try simulating and hardening sample design
- o Only ran RTL simulations, had issues with gate level sims
 - Tools crashed with gate level
 - Previous team also had gate level problems, mostly doing RTL now
- Project Ideas:
 - DSP related projects
 - Road noise suppression system
 - Voice audio boosting system
 - Similar to hands free audio in a car
 - HDMI scaler
 - Open source implications? What standard needed?
 - How much analog needed?
 - Choose a small number as a team to take to the next step
 - How difficult?

- Is it feasible?
- Can we do this?
- Want access to microcontroller area to debug
 - build in redundancies
 - Try to prove something works if full functionality not possible
 - Could look at open FPGA systems

Project Ideas

Would we be able to do three/four modularized sections with different smaller designs? Some ideas are listed below which we will start working on, but would depend on size requirements:

- 1x Hardware ALU / Compare peripheral GL
 - 2 input regs, 1 output reg, 1 control reg, daisy-chainable in hardware.
- Power and clock gating Each portion can be independently powered on- needs research
 What if it breaks? Can't test any of them. Hardware and software override
- Small DSP something audio / visual / something? WG
- Gate delay measuring circuit or similar? JH
 - Test how accurate the timing is in the tool flow
- Wishbone sanity check JH
 - Read from one register, write to the other as a sanity check to ensure the wishbone bus is working.
- Optionally Serial input/output apart from the wishbone bus using I2C as a backup muxed through the external pins for redundancy if wishbone is dead. CB

Weekly Progress

• Additional Adder added to the basic project and modified what it is adding/subtracting

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Pending Issues

- Go to slack and ask in efabless chat about gate level issues
 Try to get gate level sims working
- No spaces in file paths for caravel repository (make setup crashes)

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Team Contract	5	15
Gregory Ling	Team Contract	5	15
Will Galles	Team Contract	5	15
Cade Breeding	Team Contract	5	15

Plans for Upcoming Week

- Propose modularized project idea to Dr. Duwe (Client + Advisor)
- Keep messing with the basic adder circuit
- Start to investigate modules (size and intensity) that we decide to move forward with
- Test shared git repository with caravel template and sample adder

Meeting Questions For Dr. Duwe on Monday

- See Project Ideas section above as we have a general project proposal.
- Research main project vs playing with older projects
- FRAM is not looking well:

https://www.ti.com/lit/ml/szzt014a/szzt014a.pdf?ts=1676844479074

FRAM Manufacturing

While the benefits of FRAM have been known for many years, productization at acceptable manufacturing yields has posed challenges to many companies.TI has been *successfully* producing FRAM memory at an advanced process node (130 nm) for over two years. TI's FRAM technology is the result of *over 10 years of manufacturing development with well over 200 issued patents*.

o https://en.wikipedia.org/wiki/Ferroelectric_RAM

competition with FeRAM.

Texas Instruments proved it to be possible to embed FeRAM cells using two additional masking steps^[citation needed] during conventional CMOS semiconductor manufacture. Flash typically requires nine masks. This makes possible for example, the integration of FeRAM onto microcontrollers, where a simplified process would reduce costs. However, the materials used to make