EE/CprE/SE 491 WEEKLY REPORT 2

Digital ASIC Fabrication

2/6/2023 – 2/12/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Meet with previous senior design group (sdmay23-28) to go over testing a base adder circuit and viewing its waveforms
    - Also worked on hardening the user_adder design given to us
    - Two senior design teams behind us gave the team we met with this design, so it has been passed through multiple times now.
    - Confirmed we could view the adder in GTKWave after simulating the RTL Verilog files
- Worked on setting up out gitlab repository with all of the caravel files from a generic repository template, including the new adder files we were given
- Resources were given to us from previous team
    - https://www.zerotoasiccourse.com/: Project ideas and videos on ASIC fabrication

Meeting Notes from Previous Week with Dr. Duwe

2/6/23

Update from last week

- Figured out tools for Windows and Mac systems
- Successfully ran simulation and hardening with sample project
- Had better luck with WSL2 than CygWin
- Ran sample IO_Ports_test sim and harden

Questions to answer:

- What is feasible with the tools given?
- Should we try to use some other tools? Probably not
  - See what is offered to increase confidence before pushing to pre-check or submission
  - Have strong case on why design will work

Notes

- Once we know how everything works, project becomes better scoped and easier to submit
- Plan to look into FRAM after toolflow set up better
- How far along was previous group before deciding project/scope?
  - Not a huge priority on picking project (no set date)
  - For now keep as general scope, keep working on tool setup
  - Wider scope helps give idea on research/idea phase while starting early
  - Course will require us to give presentation and design submissions eventually, eventually forced to narrow scope
- No info on MPW7 updates as of now
  - Nothing on shipments yet

TODO:

- Make a concrete modification to an existing project, try project from 2 semesters ago
  - Add another adder, etc
  - Can it still work after changed?
  - Send more data? Update control bus? Wishbone bus
  - Can you use the logic analyzer?
  - Useful for bringup plan?
  - Can you modify the user area?
- Schedule meeting with Previous team (sdmay23-28)

Pending Issues

- Gate Level simulations
- Start to narrow down project idea

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Worked with tools, set up adder	5	10
Gregory Ling	Worked with tools, set up adder	5	10
Will Galles	Worked with tools, set up adder	5	10
Cade Breeding	Worked with tools, set up adder	5	10

Plans for Upcoming Week

- Get everyone working with the software and able to modify and simulate the basic adder project
- Finalize candidates for project.

Meeting Questions For Dr. Duwe on Monday

- Suggest a DSP related project to for overarching project idea
    - Road noise suppression from Issaac Rex
    - Other audio related project
- Image modification project idea
    - Some form of image processing
    - Build in HDMI port
    - 2 HDMI in to 1 HDMI out split screen