EE/CprE/SE 491 WEEKLY REPORT 10

Digital ASIC Fabrication

4/16/2023 – 4/30/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

- All – Finish Design Document and create Faculty Presentation

Meeting Notes from Previous Week with Dr. Duwe

4/17/23

Updates from us:

- Started compiling entire design document from the weekly sections
- Started putting together presentation
- Gregory worked on the wishbone bus
- Jake got the shift in and shift out registers working

Design Document

- Section for results and final implementation, do we need to update?
  - Section 4.5 Design Analysis
    - Should not be whether proposed design works in 4.3
    - The place to argue that our proposed design is going to meet our requirements
    - Put any evidence in there that we have
    - Say WHY it meets the requirements
    - Potential design alternatives there
    - User Area analysis with OpenRAM?

        - Section 5.8 Results
            - Add shift in and shift out register
            - Standard cell test
            - Adder simulation
        - 4.2.3 Decision making
            - Don't start with saying we didn't make any decisions
            - DSP module will have lots of tradeoffs
            - Be more accurate and honest about the decisions we did make
            - We had a lot of flexibility, so we had to make these decisions for XYZ reasons
    - For the whole document, do NOT say there were not any ethical or safety considerations
        - Reason to believe we should trust the people who make our chip and the wrapper
            - But we still do not know what we are getting fully
            - Any hardware trojans into your design?
            - Is IP leaking?
            - Make sure wrapper is secure and free of bugs (it's not free of bugs)
            - Make sure toolchain isn't messed with
            - Project not intended to be very secure, meant to backdoor

Custom Cell

- What does Duwe want?
    - Data Retention FF
        - Flip Flop that you can make go to a very low voltage and still retain the value
        - Reach out to Bryan Kalkhoff?
    - AOI cells? And, Or, Invert
        - Already exists in the standard cell library

DSP Road Noise

- Do we need to flip bits to multiply?
    - No
- Need to shift 3 bits right after multiplying instead
- If doing accumulating, may need to saturate
    - If multiply accumulate, multiply accumulate, etc then saturation needed
    - Need extra bits on the scale of log2(# of accumulations)
-

4/24/23

Updates from us:

- Design doc rev 1 is complete
- Working on presentation this week
- Practice Presentation with Duwe

        - Monday May 1st 10:00pm practice presentation with Dr. Duwe
        - Duwe may have something at 11
        - May take longer than an hour
    - Moving presentation time
        - Moving to Thursday 9-10 AM, May 4th
    - Presentation
        - Cite documentation and pictures
        - More pictures, less text
        - When figures are included, increase the font size, bold them
        - When talking about it, highlight one, user a laser pointer
    - Exit Interview
        - Tuesday May 9, 3-4pm

TODO:

    - Work on presentation this week

Weekly Progress

- Gregory – Design Document and Faculty Presentation
- Jake – Design Document and Faculty Presentation, Backdoor SPI Design specifications
- Will – Design Document and Faculty Presentation
- Cade – Design Document and Faculty Presentation

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Design Doc and Faculty Presentation	12	60
Gregory Ling	Design Doc and Faculty Presentation	10	46
Will Galles	Design Doc and Faculty Presentation	10	60
Cade Breeding	Design Doc and Faculty Presentation	10	45

Plans for Upcoming Week

Present our Faculty Presentation