EE/CprE/SE 491 WEEKLY REPORT 1

Digital ASIC Fabrication

1/24/2023 – 2/5/2023

Group number: sddec23-06

Client & Advisor: Dr. Henry Duwe

Team Members/Role

- Jake Hafele
- Gregory Ling
- Will Galles
- Cade Breeding

Past Week Assignments

ALL

- Schedule initial meeting with Dr. Duwe
- Find project ideas
- Scheduled weekly workdays on the weekends with group mates
- Start working with the Efabless p
- Get the build system set up and perform an initial simulation of the example project

Meeting Notes from Previous Week with Dr. Duwe

Initial goals:

- Get familiar with Efabless tools
- Decide what we want to do with blank core

Tools:

- Easier/faster to use local tools than remote
- Final tweaks and final precheck done on open galaxy
  - Has to run on their system to pass checks
- Docker image to run locally
- GTKWave alternates
  - Can use modelsim for waveform viewer for VHDL or Verilog models
  - Can use VCS which is Synopsys version of Verilator with school license

- Get added to Efabless slack for more resources
  - https://open-source-silicon.dev
  - Invite link to slack channel

Project Ideas:

- "Would there be any good ideas that could be put to use for other research projects?"
  - Probably not, what would the use case be to harden a chip?
  - Wireless research teams may be interested on digital end
  - Analog people build their own chips if they need to
    - If it was super critical, they would already be doing it
  - Digital teams may just build on FPGA
  - Lots of speculative questions if at research level
    - Can we put a platform down as a baseline to evaluate power, etc
- Low Power ASIC
  - How easy to measure inside caravel?
    - Worst case, see current pull and turn off parts of chip
    - Try driving Vdd pins to user areas to see effects
    - Look at clock gating, power gating, measure different techniques used
    - How well would the harness support extra measurements?
  - Could we build our own power wrapper inside of caravel wrapper?
    - Would rather have PCB with power management IC's to measure current + python scripts over SPI/I2C
- FRAM/RRAM
  - Open source RRAM macro available
  - Check availability in MPW's
  - FRAM is byte updatable flash
    - Writing is done with a bulk erase
    - Each read is destructive, have to write again after read
    - Done 1 byte at a time
  - May be too far for one project
- Matrix multiply unit with SRAM put down
  - Power gating?
  - Enough lead time to implement, not simple
  - Well developed project with power testing
- RAM Compression
  - Neural network accelerators
  - Intermittent compression?
  - Compress from DRAM to SRAM, less energy per action
  - Compression takes time and energy to undo
    - Slower to load overall, depends on constraints
    - Same with encryption
- Encryption
  - Encryption hardware may be too large

Notes:

- Core project is doing the chip fab from start to end
- Be careful on class idea of who the "user" is and purpose

        - Open source community? Research?
        - Risk mitigation with power measurement with developed PCB
    - Any size constraint issues with other teams?
        - Tyler Green said they could put 6 KB SRAM down
        - Make sure pass DRC
        - 2 or 3 could fit, 6 may be too much

TODO:

- Get familiar with the tools
    - Run example project and try to harden
- Contact other team
    - They will be working more on documentation
    - Their goal will be to have us run through their documentation/deliverables
- Research more topic ideas
- Set up time for workday

Pending Issues

- We are having issues installing the development tools on a Windows OS

Individual Contributions

- All contributions were for the group this week.

Team Member	Contribution	Weekly Hours	Total Hours
Jake Hafele	Got it set up	5	5
Gregory Ling	Got it set up	5	5
Will Galles	Got it set up	5	5
Cade Breeding	Got it set up	5	5

Plans for Upcoming Week

- Get everyone working with the software and able to simulate and test the example project.
- Finalize candidates for project.