Testing Plan

Digital ASIC Design

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Problem Statement

Problem Description

The ability to create a custom digital ASIC (Application Specific Integrated Circuit) is often limited to industry professionals and locked behind a high barrier to entry.

Goals

- Gain insight on open source designs for digital ASIC production
- Test the eFabless capabilities including:
    - Clock Gating
    - Custom Cells
    - DSP Applications

Unit Testing

- 1 Testbench for simpler modules
  - Standard cell, custom cell
- More complex modules will have more testbenches
  - Road noise filter, backdoor SPI
  - Test adders, multipliers, RAM
- Tests performed with RTL and gate level simulations

Interface Testing

Test two major busses

Wishbone bus

- Make sure that data can be transferred to and from in single chunks
- Make sure that we can stream large chunks of data sequentially

Backdoor SPI

- Make sure that we can cross the different time domains

Integration Testing

- Critical Paths include:
  - Wishbone Bus
  - SPI Bus
  - GPIO
- Each module will contain individual address space
  - Ensure each module can be addressed individually

Systems Testing

Test the full incorporated final design as one system

- Run the C test code in simulation
- Extremely slow
- Best guarantee our project will work as expected during testing after it is returned.

Regression Testing

Submodules are separate entities

- New submodules should follow this principle
- Existing ones should still be able to pass its submodules tests for functionality as well as any tests for new functionality

Acceptance Testing

- Verify RTL and gate level simulations with expected output
- Testbenches designed to test all functionalities of the submodule
- Keep submodules separate from each other

What questions do you have?