Requirements, Constraints, and Engineering Standards

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Problem Statement

Problem Description

The ability to create a custom digital ASIC (Application Specific Integrated Circuit) is often locked behind high barriers to entry and restricted to industry professionals.

Goals

- Gain insights on the open source design availabilities
- Test the eFabless capabilities including:
  - Clock Gating
  - Power Managment
  - Custom Cells

Intended Users and Uses

- Future Design Groups
  - Learn the process and limits of designing an ASIC chip
- Research Teams
  - Create low cost ASIC circuits for research projects
- eFabless Open Source Community
  - Utilize components to create more complicated design without designing from scratch

Requirements & Constraints

- eFabless Open MPW (Multi-Project Wafer) submission requirements
- Caravel Harness Directory Structure Requirements
- Test the limits of the eFabless process to the best of our ability
- Include a bring up plan for future team to test manufactured design once returned
- Test and verify functionality of previous team's manufactured design

Engineering Standards

- Skywater 130 nm manufacturing process
- Verilog language (IEEE 1364-2005)
- C language (c11 standard)
- Serial Peripheral Interface (SPI) protocol
- Universal Asynchronous Receiver and Transmitter (UART) protocol
- Wishbone Bus
- Inter-Integrated Circuit (I2C) protocol