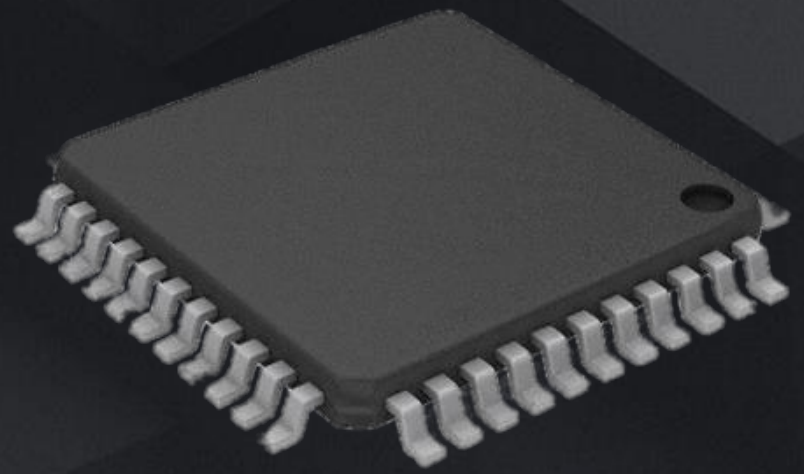

Design Plan

Digital ASIC Design

sddec23-06

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Class: CPR E 491
Advisor: Dr. Duwe

Problem Statement

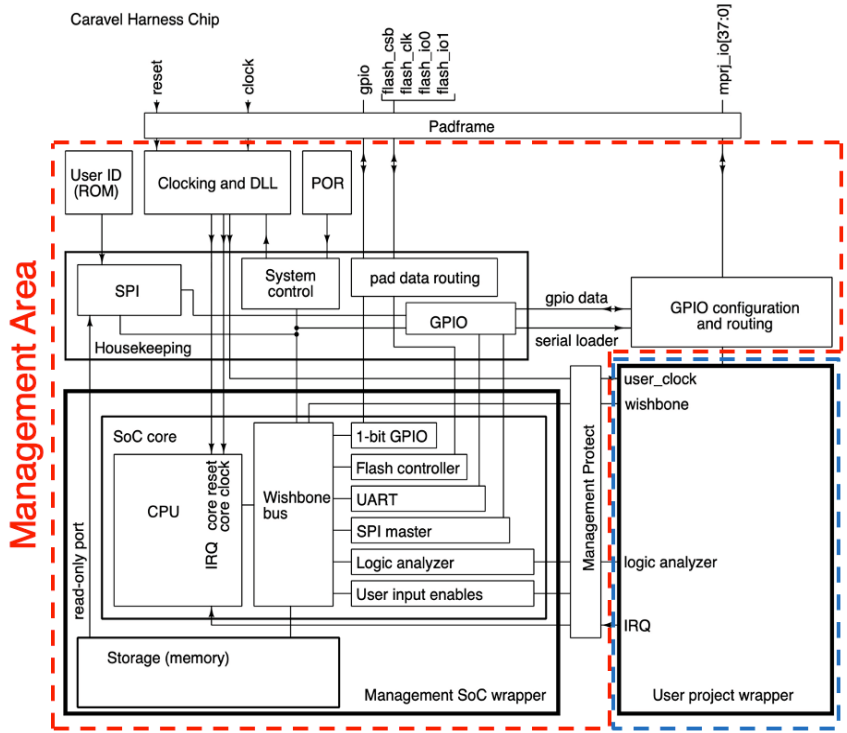
Problem Description

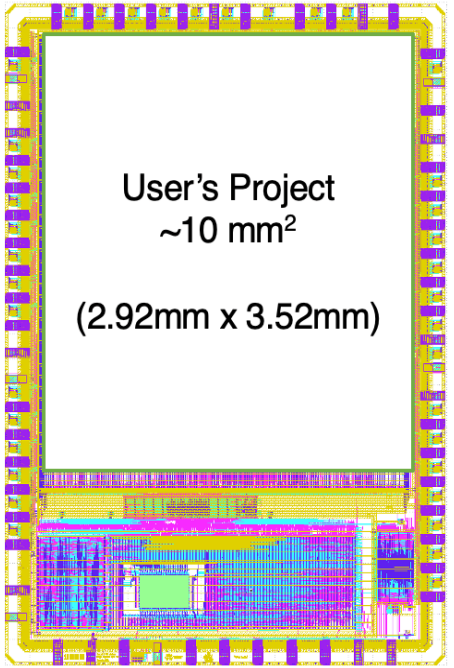
The ability to create a custom digital ASIC (Application Specific Integrated Circuit) is often limited to industry professionals and locked behind a high barrier to entry.

Goals

- Gain insight on open source designs for digital ASIC production
- Test the eFabless capabilities including:
    - Clock Gating
    - Custom Cells
    - DSP Applications

Overview Diagram





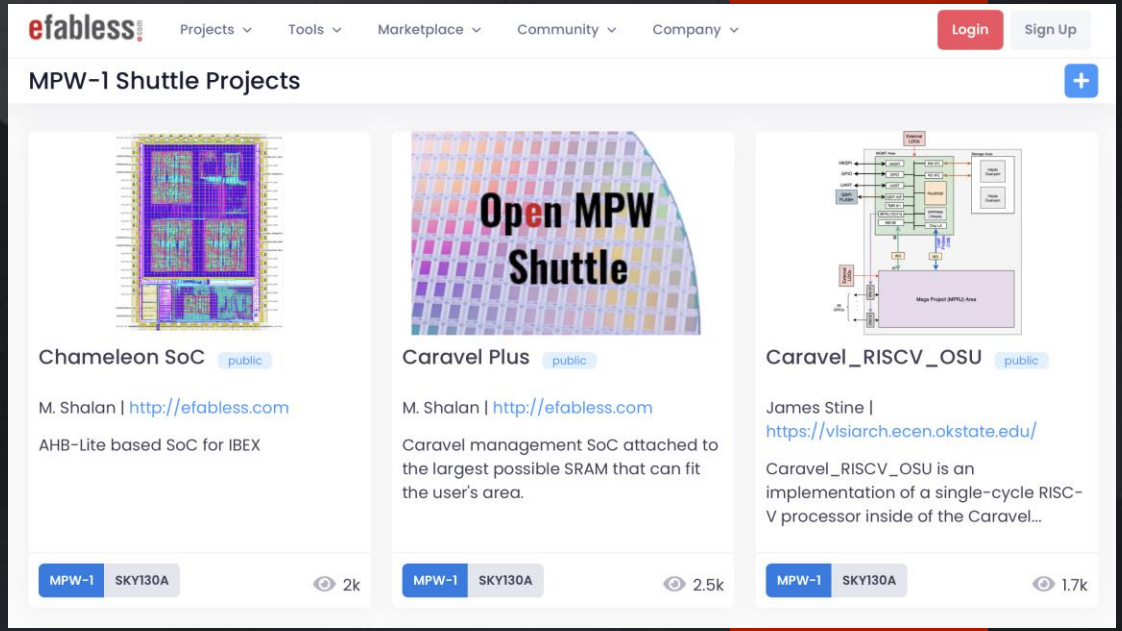
Design Context

User Needs

- Future Design Groups
- Researchers
- Open Source Community
- Our Team

Prior Work/Solutions

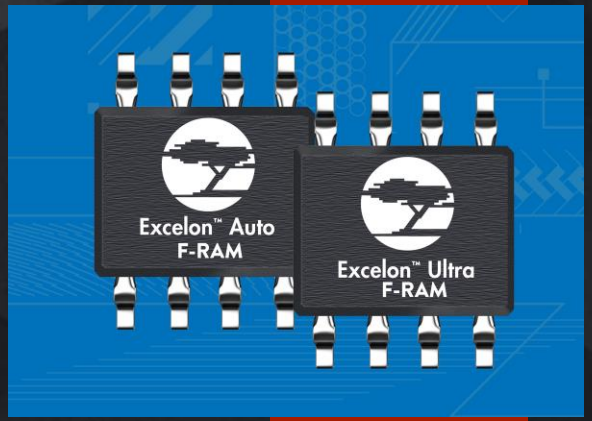
- MPW-1 Shuttle
- Caravel Documentation
- Prior Senior Design Teams



Design Exploration

Design Decisions

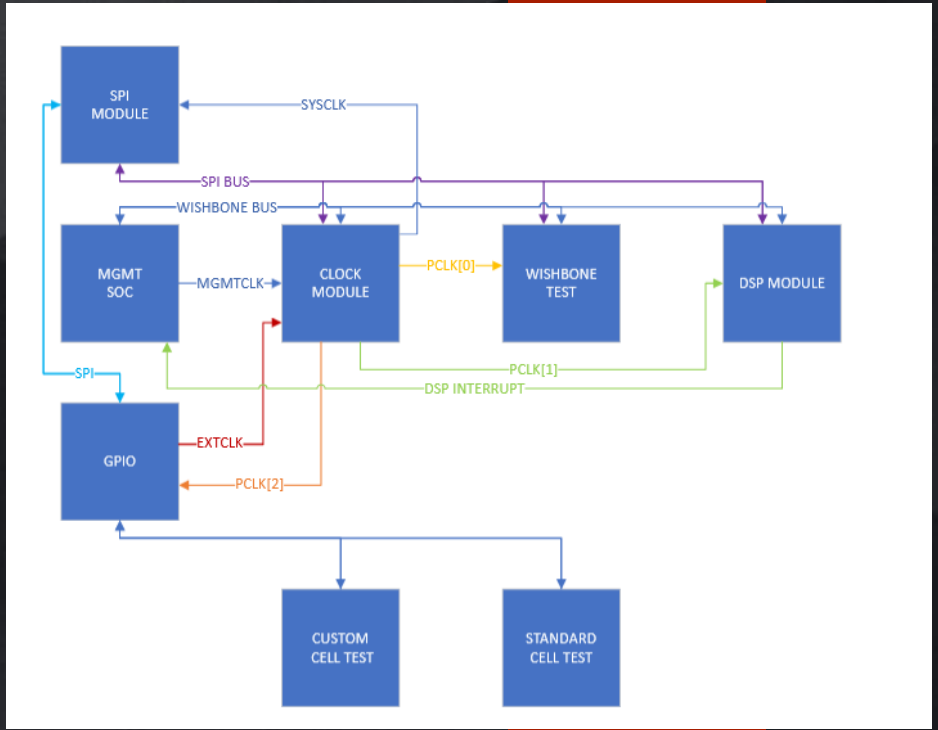
- Modular or one design?
- How can we reduce the overall risk of chip failure?
- Submodule Ideas that wouldn't work?
  - Power Gating
  - FRAM
  - Neural Network DSP Filter



Proposed Design

Modular Design

- Voice Road Noise Isolation
- SPI Interface
- Wishbone Test
- Standard Cell Test
- Custom Cell Test



Design Analysis

Current Progress

- Met with previous team to go over RTL simulation
- Investigated Skywater Standard Cell libraries
- Decided which modules to implement
- Investigated how best to implement Voice Road Noise Isolation
- Explored creating a custom logic cell
- Created detailed explanations of each module in our design specification document

FAQ

Why use this framework?

- To explore what is possible in the eFabless fabrication process. Fabricating a chip usually costs >$50,000. eFabless is free and funded by Google.

Who's going to use it?

- Future senior design or research groups who would benefit from free ASIC resources and having the confidence their design will work when returned from fabrication

Why not make something flashy like a 3D accelerator?

- While making a 3D accelerator might be fun, our goal is to test the limits of the system, and a single large design will not fulfill the design goals as well as smaller dedicated tests.

What questions do you have?